Core Power Delivery Network Analysis of Core and Coreless Substrates in a Multilayer Organic Buildup Package

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Abstract

The use of flip chip organic buildup substrates is a popular choice for large Application Specific Integrated Circuits (ASICs) due to the high routing density they offer at a relatively reasonable cost. A typical buildup package consists of multiple high density routing layers (buildup layers) supported by a thick core. The laminate core adds rigidity to the substrate and can be configured to various thicknesses such as 400um, 600um and 800um.

Coreless substrates are an emerging technology targeted to increase the routing density, lower the package z-height, while providing better electrical performance. This is primarily due to the replacement of thick core layers with a thin buildup layer. As the trend for higher levels of performance and system bandwidth continues, coreless technology is well positioned as an enabling technology solution.

In this paper we compare the performance of the core power delivery network (Core-PDN) of two 31mm, 900 ball, 8 layer organic flip chip buildup substrates. We first analyze the substrates in the frequency domain and then evaluate the transient response under various switching conditions. Both packages are designed identically except for the core versus coreless substrate construction.

Two-port high frequency S-parameter measurements between 50MHz and 2GHz are carried out using a Vector Network Analyzer (VNA) to characterize the PDN in the frequency domain. Both simulated and measured data are correlated in the frequency domain. Time domain response of PDN to current transients with various switching conditions are simulated and presented.

I. Introduction

Integrated circuit performance is highly related to the robustness of power distribution networks. Circuit timing and jitter characteristics are a strong function of noise on the power supply. The power integrity degradation due to switching current of the core logic circuits through the impedance of the Core-PDN critically impacts the performance of high speed digital systems.

With increasing clock speeds and decreasing voltage levels, the acceptable noise margins on the PDN continue to shrink. This trend necessitates robust PDN design and analysis to ensure acceptable system level performance.

The impedance of the power distribution network significantly accounts for core noise. Some of the critical parameters that impact the impedance of the PDN are the impedance of vertical interconnects such as vias, bumps, solder balls and the horizontal interconnections such as power/ground plane pairs, their separation and the properties of the dielectric medium between them.

Typical core thickness of laminate buildup packages are primarily 800um, 400um or to a lesser degree, 600um in single core configurations. Depending on the PDN performance requirement, multiple core constructions of alternating power and ground planes could also be utilized to achieve lower impedance configurations, although they would add to the overall layer count, complexity and cost of the substrate.

There is a rapidly growing need for thin core substrates (<400um) that support thinner die for next generation electronic products such as tablets. Coreless technology is a viable solution to reduce the overall package height, layer count and to improve package electrical performance. This is achieved by replacing the thick core or multiple cores consisting of thick glass-resin dielectrics. Figure 2(a) shows a conventional dual core substrate and Figure 2(b) shows a coreless substrate which results in a significantly thinner package.

Figure 2(a). A 12 layer, dual-core buildup package with total package height of 1.712mm

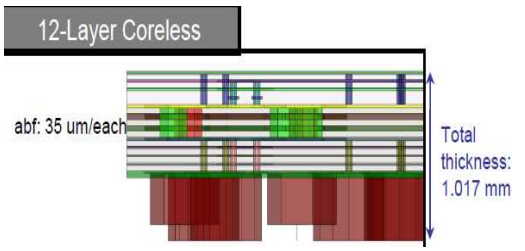

Figure 2(b). A 12 layer coreless substrate with total package height of 1.017mm.

In a typical thick core configuration, the thin buildup layers (routing layers) are constructed symmetrically on both sides of the core resulting in a package construction such as 3-2-3, 5-2-5, 3-4-3. Figure 3 shows a cross section of a typical 5-2-5 construction.

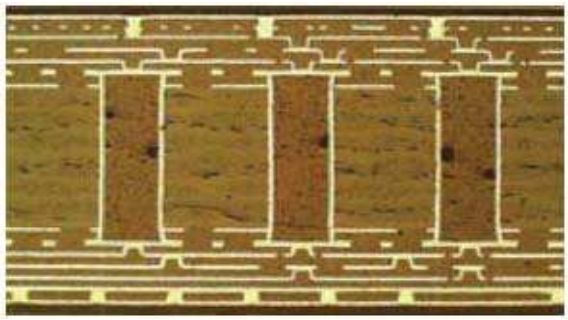

Figure 3. Equal number of buildup layers above and below the core are primarily for copper balancing intended to improve package mechanical stability.

The symmetrical construction above and below the core layer balances the metal percentage to ensure good mechanical stability. This approach results in redundant buildup layers below the core that may not used for additional routing. High Volume Manufacturing (HVM) design rules of 25um line/space typically provides adequate routing density to accomplish routing above core layers in a microstrip or stripline configuration. Coreless technology eliminates the requirement of symmetrical construction. A substrate design with fewer layers below the core ultimately may result in a lower cost package while improving electrical performance. Furthermore, the power and ground planes can be placed in any layer providing additional design flexibility.

The primary advantages of coreless technology can be summarized as follows:

- Stackup Flexibility
  - Symmetrical stack-up is not required,
  - Layers may be reduced,
  - Cost may be reduced due to elimination of substrate layers.
- Via size reduction
  - Large plated through-hole (PTH) vias found in substrates with thick cores are replaced with microvias, resulting in dramatic via size reduction. Via size reduction, in turn, increases routing density.

Table 1 illustrates the significant difference in substrate real estate usage between PTH and microvias.

	Capture Pad (µm)	Drill Size (µm)
PTH Via (400µm)	350	200
Micro Via	100	50

Table 1: Capture pad/ drill diameter of PTH versus microvias.

  - Reduced crosstalk between vias due to flexible via placement and shorter via barrel length.
- Thinner package
  - Shorter vias between layers with less parasitics. See parasitic inductance comparison in Table 2.

	Inductance (nH)
PTH Via (400um)	0.14
Micro Via	0.01

Table 2: Self Inductance of PTH via versus microvia.

  - Lower PDN impedance due to the lack of a core,
  - Lower IR drop,
  - Lower power consumption,
  - Potential elimination of decoupling capacitors.

II. Probing and Measurement

The two packages characterized are 31mm, 900 solder ball, 8 layer fcBGA packages.

For characterizing the PDN impedance, the required samples are the bare package substrates. The probing is performed on the power/ground bump pairs using a two-port VNA setup. The top solder mask layer of both package substrates was removed for the flexibility of using probes with a larger pitch than the bump pitch. Figure 4 shows the measurement site.

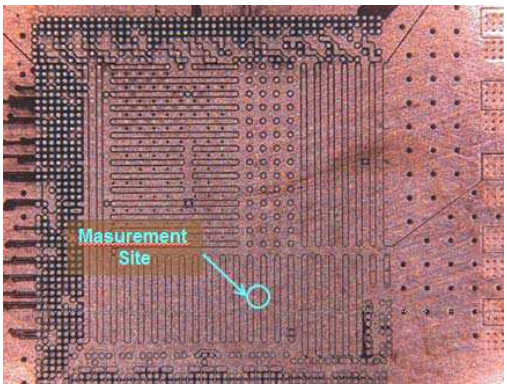

Figure 4. Top soldermask layer of both packages are removed to access the measurement site.

An Agilent 8720D Network Analyzer with 250 um pitch, 50 Ohm ground-signal-ground microprobes was used. The calibration of the Vector Network Analyzer was performed using a standard open, short, loop-through (OSLT) method over the frequency range of 50MHz to 2GHz. The power/ground structure can be easily probed from the bump location since there are numbers of power/ground pairs available. The impedance of the PDN can be measured by this method from the die side bump locations. The two probes contact the same pair of power/ground pads as depicted in Figure 5.

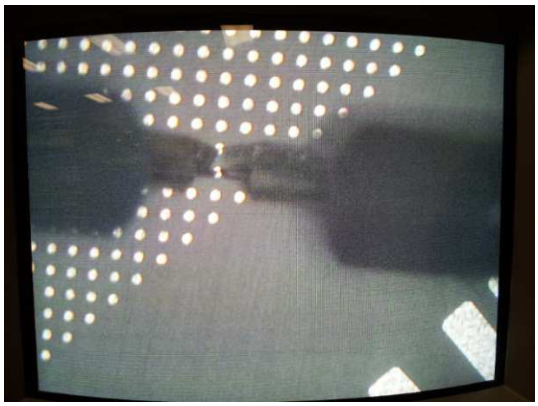

Figure 5. Microprobing of ground/power bump pair.

The two-port measured S-parameter data is then converted into the impedance of the plane pair. This approach is described in the paper of Istvan Novak [1].

To prepare the samples for measurement, the BGA side of the packages were painted with a conductive epoxy as in Figure 6. The epoxy shorts the power/ground pads on the BGA side. This method enables loop inductance extraction of the power/ground plane pair from the short-circuit impedance measurement.

Figure 6. Conductive epoxy is used to short power/ground (VDD-GND) pads on the BGA side.

III. Electrical Analysis of Power/Ground Structure

The same site was probed across three samples, labeled as Sample A, B and C for both core and coreless packages to ensure repeatability within manufacturing tolerances. In addition to the measurements, data was simulated for both packages using a commercial 3D solver such as PowerSI from Cadence. The package design database was imported directly into the 3D simulation environment. The substrate vendor's material properties and the actual package design was used to build the simulation model. The ports were set up to emulate the measurement environment.

The short circuit impedance of the power/ground structure can be read directly from the VNA. The results of the measured data and its correlation with the simulation for both the core and coreless substrates are depicted in Figures 7(a) and 7(b). Excellent agreement between simulation and measurement is observed.

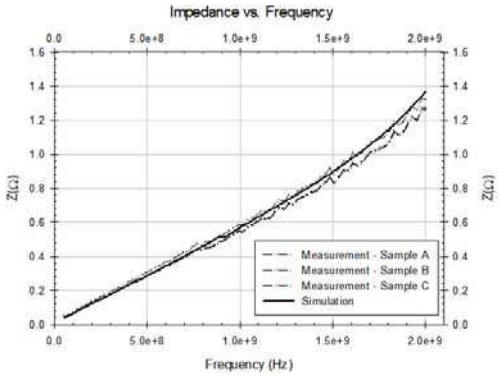

Figure 7(a). Measured versus simulated short circuit impedance of the core substrate.

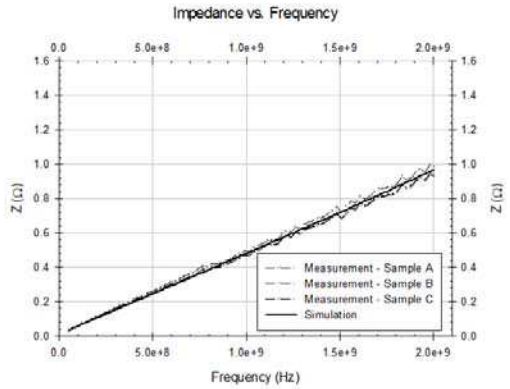

Figure 7(b). Measured versus simulated short circuit impedance of the coreless substrate.

Figure 8 shows the comparison between core and coreless impedance measurements.

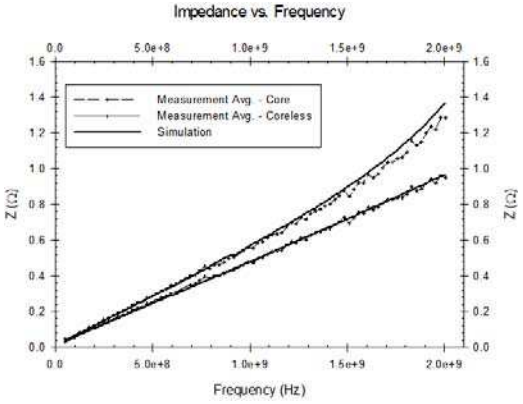

Figure 8. Short circuit impedance comparison between core and coreless substrate

Clearly, the impedance of the coreless substrate is lower across the measurement band. The difference is more pronounced above 1GHz. From the short circuit impedance measurement, loop inductance can be extracted and is shown in Figure 9. As expected, the coreless substrate is less inductive, primarily due to tighter coupling between the power and ground plane pair as well as the replacement of highly inductive core vias with microvias. Loop inductance of the coreless substrate was extracted to about 75pH versus 96pH in the core case. A difference of roughly 20%.

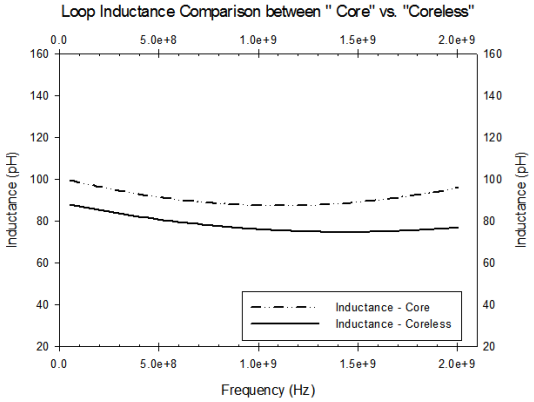

Figure 9. Coreless substrate loop inductance is 20% lower.

IV. Time Domain Analysis of Core PDN

For the system engineer the inductance or the impedance of the Core-PDN is an important performance parameter. However, the ultimate measure of PDN robustness is the noise voltage induced on the VDD pins due to core-switching activity. Typical acceptable noise margin is 5-10% of the core VDD. To understand the noise margin, we setup a simple circuit as shown in Figure 10. A peak current of 1.5 amps is modeled through a piecewise linear source with edge rates of 150 psec and 300 psec. DC Voltage of 1.1 V is applied at the package balls. A 3D commercial software tool such as Cadence Speed2000 is used for this simulation. A total of 374 die side power and ground bumps as well 59 BGA side power and ground balls are lumped together in the simulation environment for the time domain analysis.

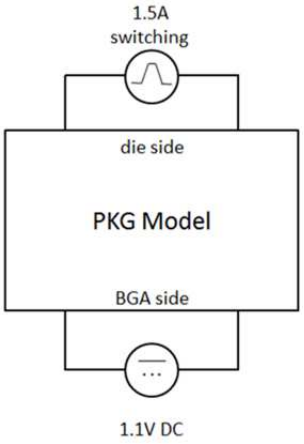

Figure 10. Simulation model to assess induced noise voltage due to core switching activity.

The current stimulus corresponds to 1.33GHz for 150 psec edge rate and 655 MHz for 300 psec edge rate. The current profile used in the simulation is displayed in Figure 11. We chose two different switching frequencies to evaluate the Core-PDN response under "Slow" (150psec) and "Fast" (300psec) conditions.

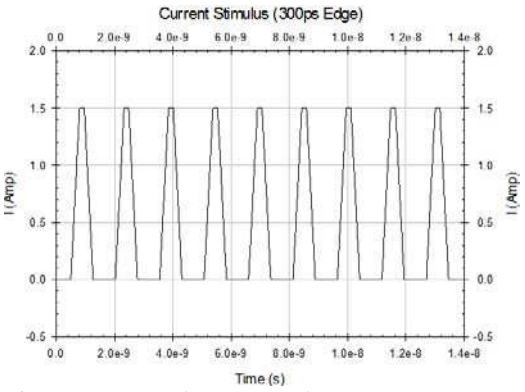

Figure 11. A 150 psec and a 300 psec current stimulus is applied at the substrate die side bumps. The 300 psec stimulus is shown.

Edge rate and current profile were chosen to illustrate the Core-PDN performance difference between core and coreless substrates. The real world switching profile could be quite complex and substantially time varied with transistor on-off cycles not necessarily being periodic. For the purpose of this study, a simple on-off profile is adequate to illustrate the behavior of PDN and compare both substrates.

The response of PDN for both core and coreless substrates to on-die switching activity is displayed in Figure 12(a) and 12(b).

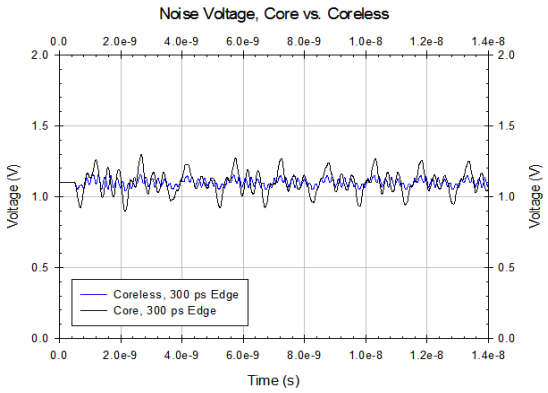

Figure 12(a). Core-PDN response to Slow edge.

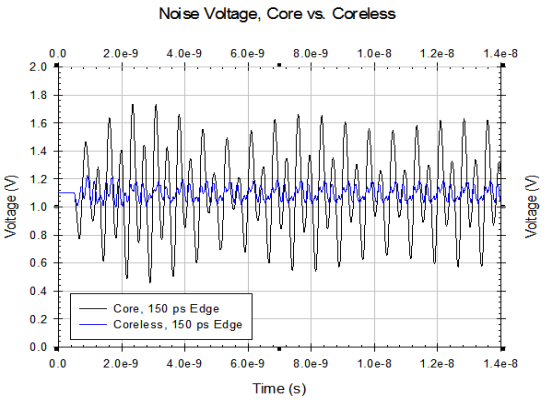

Figure 12(b). Core-PDN response to Fast edge.

Worst case peak to peak noise voltages are listed in Table 3.

	Noise Voltage, V_{Np-p}	
	Slow (300ps)	Fast (150 pS)
Core	340 mV	1240 mV
Coreless	100 mV	200 mV

Table 3. Comparison of noise voltage (V_{Np-p}) between core and coreless substrate.

The nominal supply voltage is 1.1 volts. The worst case noise voltage is calculated at +/- 56% of the nominal supply voltage in the case of the core substrate and +/- 9% for the coreless substrate. The data suggests that as the frequency of operation increases, the coreless technology provides significant noise margin improvement compared to core version particularly beyond 1 GHz. This outcome is expected and can be primarily attributed to the lower impedance of the PDN as seen by the silicon.

IV. Summary and Conclusion

We demonstrated both qualitatively and quantitatively the unique advantages coreless technology provides with particular emphasis on Core-PDN performance. Our simulated and measured data shows significant margin improvement that would result in better system performance with coreless technology. Z-height reduction, potential layer count reduction, increased routing density and better electrical performance positions coreless technology as a viable solution to meet the demands of next generation electronic products.

References

[1] Istvan Novak, "PicoHenrys in Power Distribution Networks", DesignCon 2000.

[2] GaWon Kim, SeungJae Lee, JiHeon Yu, GyuIck Jung, JinYoung Kim, Nozad Karim, HeeYeoul Yoo and ChoonHeung Lee , "Advanced Coreless Flip-chip BGA Package with High Dielectric Constant Thin Film Embedded Decoupling Capacitor", in proceedings of 2011 Electronic Components and Technology Conference, pp. 596-600.