Enhancing Overall System Functionality and Performance with the Right Packaging Solutions

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Abstract

Printed circuit boards (PCBs) are the essential parts to assemble modern electronic circuits. The PCB design and development process has a direct impact on the system cost and time to market. On average, companies report that PCB represents 31% of the overall product cost. Today's electronic circuits and PCB designs are extremely complex. Multi-level mistakes are inevitable during the design and development stages. Cost reduction pressure is also limiting the designers in achieving their goals by reducing a few layers from their PCB stackup or adjusting and tweaking their designs. A paradigm shift in PCB design is underway through partitioning and modularizing the system and circuits to reduce PCB size and complexity, shortens design to market time, and simplifies the overall supply chain.

In order to develop a superior product to fulfill a desired functions, good balance needs to be achieved among competing factors such as performance, cost, form factors, manufacturability, design, system flexibility, and supply chain management (Fig 1). A wireless system is usually comprised of several subsystems performing different functions. For example, a typical handset system includes baseband, transceivers, main and diversity FEM, memories, power management, power amplifiers, antenna switch, duplexer filter, etc. In this day and age, system integration is mandatory in order for end use products to offer superior and competitive products

Compared to an SoC solution, system level integration at the packaging level may provide benefits such as cost effectiveness, flexibility, and a shorter development cycle. A concurrent development methodology between device and package design will definitely help the industry to understand the nature of system integration on a package

Keywords

wireless system, SiP, System-in-Package, Module, System Integration, system size reductions, copper pillar, packaging solutions, system cost reduction, PoP, TMV, conformal shielding, Integrated Packaging Device (IPD), 3D packaging, 2.5D packaging.

Introduction

Remarkable changes are happening to wireless technology through miniaturization, integration and innovation in both integrated circuits (IC) and packaging in order to meet on going challenges of greater functionality, higher performance, smaller size, lower cost, and faster time to market. To achieve these objectives, SoC and SiP packaging technology must complement each other in order to enhance overall system functionality and performance.

Integration of complete systems of RF/analog/digital functions in a single-chip SoC is facing many obstacles due to the system requirements for high capacity memory devices, duplexer and filter banks, MEMS, high Q Integrated Passive Devices and other multimedia devices. The market demands that these features be delivered in innovative form factors. In response, 3D packaging is experiencing high growth in new applications by delivering the highest level of silicon integration and area efficiency. To achieve design flexibility and cost objectives, cell phone designers have turned to stacked die, SiP module, 2.5D and PoP packaging to solve their analog, Digital, & RF integrated circuits, antenna, passive component, and memory integration challenges. These package integration solutions must pass board level solder joint qualification, wireless device drop test, and all other mechanical rigidity and thermal requirements.

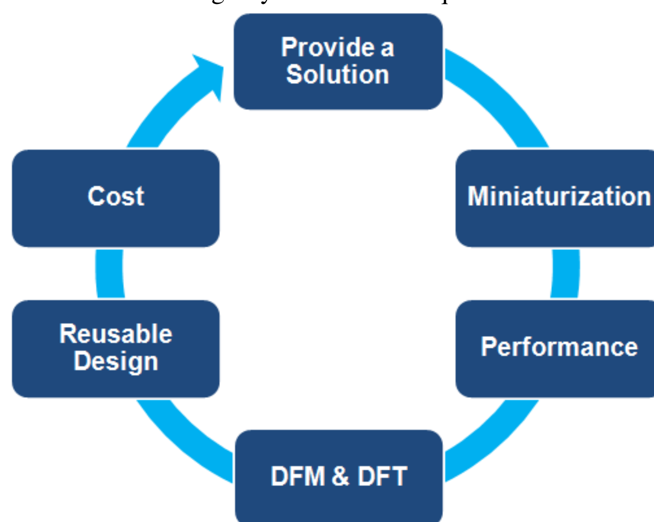


Fig. 1 – System Integration with Good Balance

A new design methodology is needed to partition different segments of the system functionality and to isolate them from coupling among different circuit segments while protecting the components from EMI interferences and noise susceptibility.

In this paper, we have proposed a system design methodology in which an effective wireless system design could be achieved when the right packaging solutions are adopted through collaboration and co-design of system, packaging, substrate, and other active/passive components.

Using a typical wireless system as an example we will explain the process of the system design methodology. How a wireless system is analyzed and partitioned in accordance with system requirements and available discrete devices; how various packaging technologies are applied to meet

performance, miniaturization and cost requirements; what are the considerations when integrated packaging solutions are developed including overall cost, performance improvement, known good die issues, design for manufacturing, design for test, reusability, etc.

Compared to the SoC solution, system level integration at the packaging level may provide a more cost saving, more flexibility, and shorter development cycle for system companies to come up with a superior product with better characters.

Wireless System and System Integration

Fig. 2 depicts a wireless system that includes a handset system and a base station system. In a typical OEM business practice, a system company (no matter on the handset side or on the base station side) designs a system PCB board, purchases discrete components from Integrated Device manufacturing (IDM) and fabless companies, and assembles the products at electronic manufacturing services (EMS) companies. This business model identifies some issues that compete for system size and system cost reductions.

Extensive competition in the wireless communication marketplace is forcing the system companies to integrate their products with greater functionality, higher performance, smaller size, low cost, and faster time to market. It is obvious that system integration is a must to achieve this solution. However, only optimized integration for a system or subsystem can provide good balance of the mentioned goals (Fig.1). Effective system partition requires good understanding of the system, the availability of needed components, and the appropriate packaging technologies. It is usually achieved by collaboration among System companies, component companies and packaging companies.

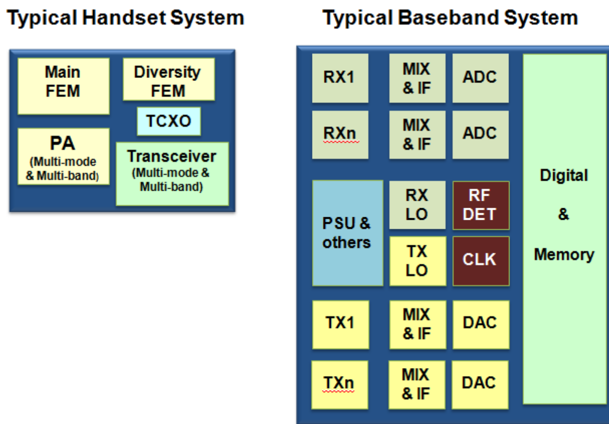


Fig. 2 – A Wireless System: Typical Handset and Base Station

Both SoC and SiP solutions can be used in a system or a subsystem and they should complement each other in order to enhance overall system functionality and performance.

Advance technologies such as PoP (package on Package), copper pillar and (TSV) Through Silicon Via, Integrated Passive Devices, and conformal shielding allow for more possibilities for system integration.

Partition of Wireless System

Fig. 3 is a demonstration of basic functional blocks in a handset system, and Fig. 4 includes basic functional blocks in a wireless base station.

It is very important to focus on generating effective subsystem solutions as a part of the integrated functions. A single or multiple subsystems can be designed into a SiP module to improve performance, size reduction, possible cost reduction, and to simplify board design interconnects.

Another important factor to consider is KGD (Known Good Die) application and availability. KGD is the key for successful SiP component development and production. How good is KGD will affect the production yield directly. For example, if a SiP Module contains 8 KGDs with 99% yield factors for each component, then overall yield for the SiP will diminish to 92.27% without considering yield loss from other factors. In order to provide high yield KGD, wafer probing and wafer level burn in are used to identify functional and infant mortality failures. Some functional testing involving RF signals are very difficult to be performed at wafer level, resulting in higher testing costs. KGD availability answers the question of which chip provider should be involved in the SiP development, and what level of KGD they would like to provide.

The complexity of developing the SiP module also needs to be controlled by considering other factors such as development cycle, testing, thermal management, RF shielding and reliability, etc. In the handset system described in Fig. 3, 1 to 4 SiP solutions can be considered. For example, one simple SiP can include only baseband and memory. And a more complex SiP can include baseband, memory, and main and diversity FEM.

For the base station transceiver system (Fig. 4), a possible system partitioning could include 4 types of SiP modules,-transmitter and feedback circuits for multiple band SiP, receivers for multiple band SiP, power management SiP, Digital and memory SiP (Fig. 5).

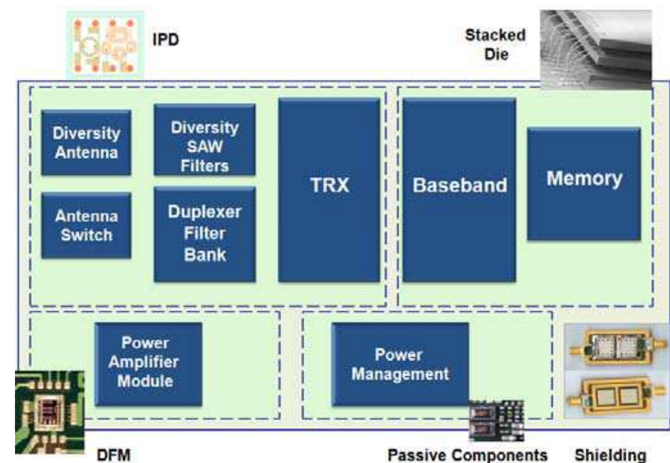


Fig. 3 - Handset SiP System Integration

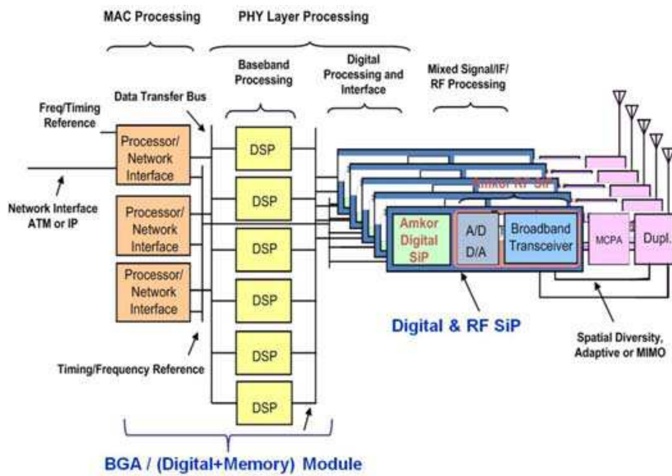


Fig. 4 – A Base Transceiver System

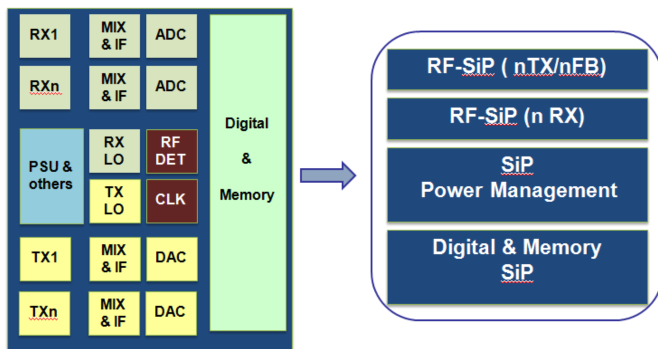


Fig. 5 – SiP Solutions for a Base Transceiver System

Packaging Technologies Supporting SiP Development

The variety and advances in packaging technology provides many possible packaging formats for system companies to develop an appropriate SiP for their specific product.

Fig. 6 and Fig. 7 illustrate some SiP solutions with different packaging formats. For example, the GPS hybrid stack is a 8.0mmx6.5mm body size; 50 lead LGA, with a flip chip base band chip, a wire bond RF chip, one crystal, one saw filter, and few passives. Another example is the ASIC with memory SiP which improves the system performance, and helps to reduce layer counts of mother board design.

The latest packaging miniaturization trend enables broader applications of SiP for system companies. Fine pitch everything practice (Fig. 8) allows wire bonding pad pitch around 50µm, flip chip bump pitch less than 50µm though copper pillar technology, substrate line/space less than 15µm/15µm, etc. On the other hand, thin everything practice (Fig. 9) adopts thinner dielectric and metal layer substrate, or thin core or coreless substrate, makes die as thin as 50µm, allows low profile wire loop (around 50µm) and thin mold cap (around 100µm) for wire bonding assembly, and permits low profile embedded shielding with conformal shielding technology. 3D chip stacking is also key for packaging miniaturization in terms of assembly technology. Fig. 10 illustrates some stacking technologies currently available - wire bond, hybrid, PoP, and (TSV), etc.

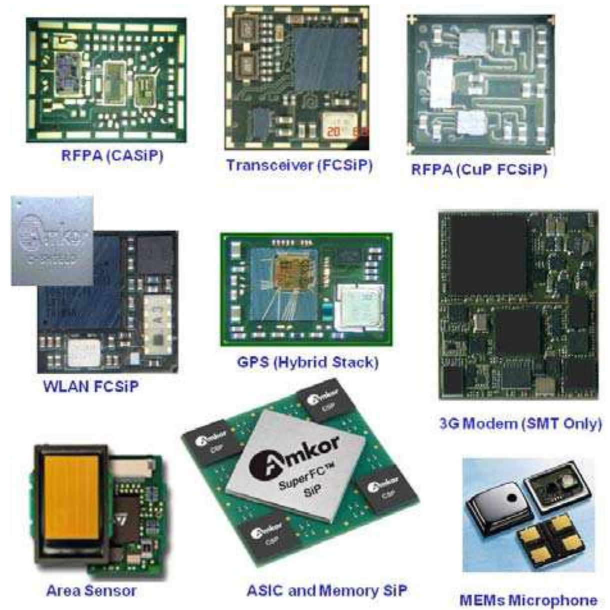


Fig. 6 - SiP Examples (1)

Additional advanced packaging technologies that enable good system integration are discussed further in more detail next.

PoP (Fig. 11) is a very popular 3D stacking technology for system integration. Customarily, a system company purchases a main component such as base band, or application processor, in PoP bottom package format. They would also purchases another related component, such as memory, in PoP top package format and then assemble them together during mother board assembly process.

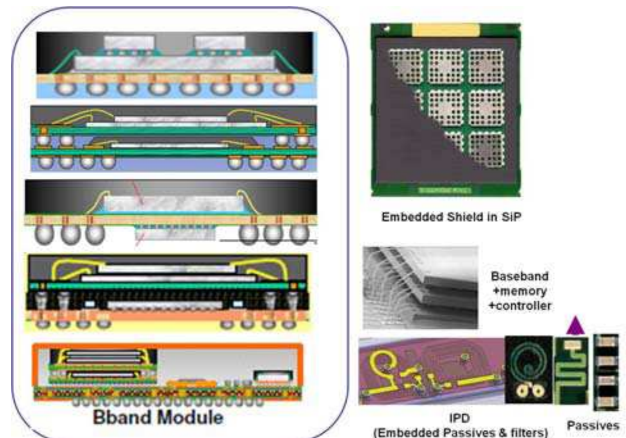


Fig. 7 – SiP Examples (2)

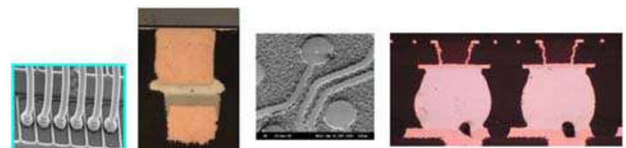


Fig. 8 – Fine Pitch Everything

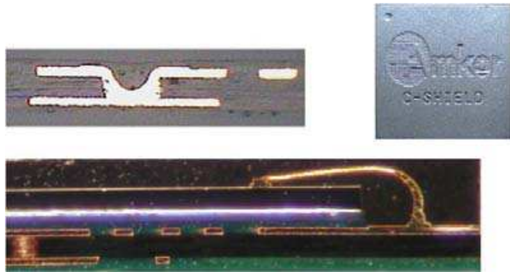


Fig. 9 – Thin Everything

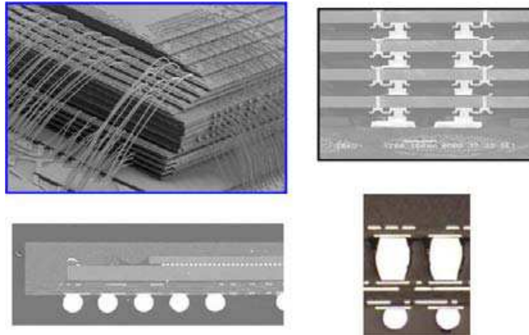


Fig. 10 – Stacking Technology Examples

Compared to conventional 3D die stacking technology, PoP structure has slightly larger packaging configuration. It allows company to choose from multiple component supply sources, and allows individual packaging testing for both bottom and top package to ensure greater flexibility and cost benefits in the system integration. PoP has proven to be a very cost effective packaging format for system integration.

To further take advantage of PoP technology, a system company may collaborate with IDMs and packaging companies to integrate more functions in either top or bottom package of the PoP, such as integrating a base band chip and an application processor chip together to meet its market needs.

TMV (Through Molding Via), Fig. 12, is an enhanced interconnecting technology with molding for PoP bottom package. The over molding can achieve less package warpage, larger die size, and finer top package interconnect.

Fig. 11 – Conventional PoP

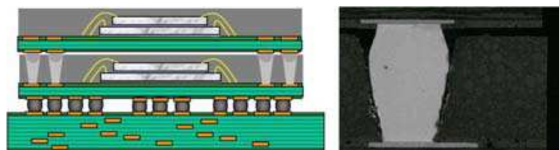
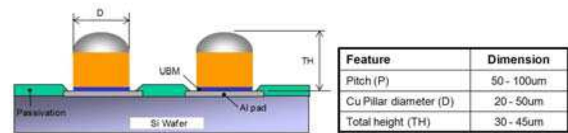


Fig. 12 – PoP with TMV

Copper Pillar is formed by a wafer level bumping process that comprises sputtering seed layer, coating resist, expose and develop resist, plating copper and solder, striping resist, etching seed layer, and reflowing solder. Typical copper pillar parameters are depicted in Fig. 13.

Conventional solder bump flip chip has the pitch limitation of about 150μm due to its reflow characteristics. Copper pillar bump can be used when fine bump pitch is required.

One of the advantages about copper pillar bump technology is its capability to use wire bond designed chips without RDL or redesign, which may result in higher performance, and size reduction (Fig. 14). Compare to an area array flip chip, a fine pitch perimeter flip chip using copper pillar, lower layer count substrate or coarse line/space are usually expected and results in a low cost substrate application (Fig. 15). NCP (non-conductive paste) is usually used as underfill for copper pillar chip assembly. A TC (thermal compression) process is used for the Cu Pillar assembly, and resulting much higher bump reliability.



Feature	Dimension
Pitch (P)	50 - 100um
Cu Pillar diameter (D)	20 - 50um
Total height (TH)	30 - 45um

Fig. 13 – Typical Copper Pillar Parameters

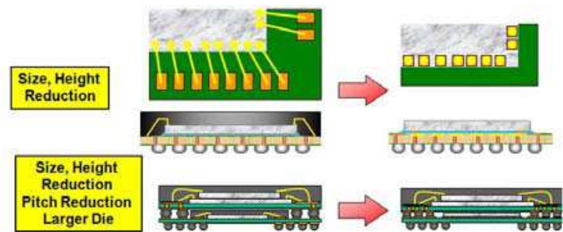


Fig. 14 – Wire Bond Chip to Copper Pillar

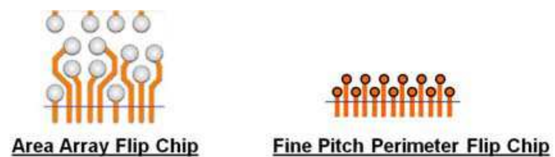


Fig. 15 – Area Array Flip Chip to Perimeter Copper Pillar

The application of Wafer level CSP in a SiP reduces the yielding loss contributed by bad Known Good Die. For low IO count chip, fan-in WLCSP can be used, and for high IO count chip, fan-out WLCSP can be used. WLCSP is a good solution when multiple bare dies are involved in system integration, Fig. 16.

TSV enables interconnects between front side and back side of a silicon chip through formed and filled vias. When TSV is used in 3D stacking, multiple chips can be stacked by TSV without wire bonding application, which ensures high performance of interconnect and small size. Fig. 17 demonstrates the migration from stacked CSP to TSV.

2.5D TSV involves a silicon interposer with TSV applied. When silicon chips are assembled on an organic substrate with flip chip technology, reliability of bumps interconnects during assembly and product life is usually a big concern due to CTE mismatch between the chip and the substrate.

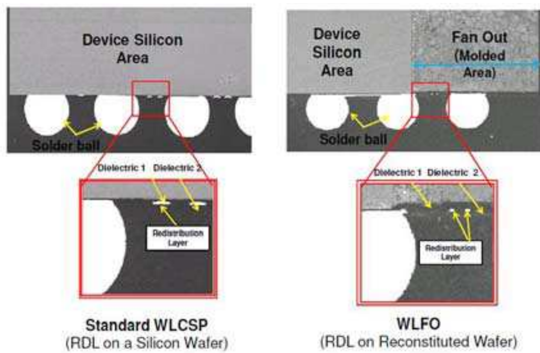


Fig. 16 – Wafer Level CSP, Fan-in and Fan-out

The situation worsens when chip size is larger and bump pitch is finer. Replacing the organic substrate with silicon substrate can significantly improve the reliability to less or no CTE mismatch, and TSV can also improve the interconnect performance.

2.5D TSV interposer has fine pitch interconnects on the top side upon which multiple fine pitch chips are assembled. The system integration is then realized through the silicon interposer and the system IOs are lead to the bottom side of the interposer through TSV. The IO pitch at the bottom side of the TSV interposer is much larger than that of the top side of the TSV thus allowing reliable assembly to an organic substrate. Fig. 18 demonstrates the application of the TSV silicon interposer. Again, silicon interposer enables greater high interconnect performance.

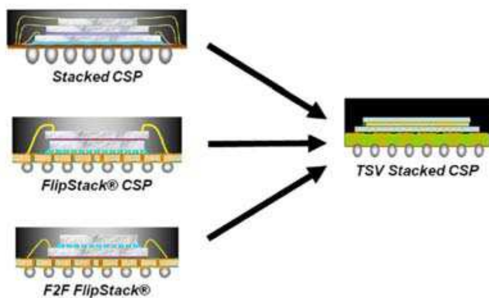


Fig. 17 – Stacked CSP to 3D TSV Stacking

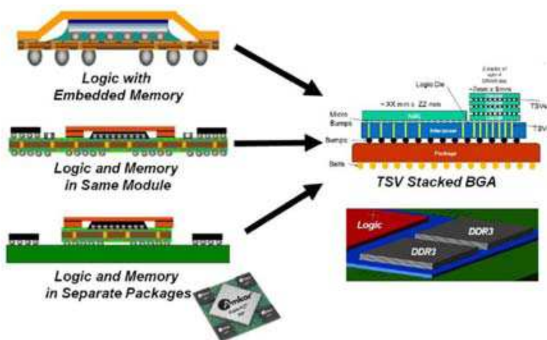


Fig. 18 – Application of 2.5D TSV Interposer

Other technologies for system integration include conformal shielding and IPD (Integrated Passive/Active Device) technologies. Conformal shielding makes EMI shielding by spraying conductive coating material over the package and realizes size reduction by eliminating embedded metal shield can (Fig. 19). IPD is fabricated on silicon or glass and is used to create functions, such as filters, baluns, diplexers, matching circuitries, de-cap capacitors, etc.

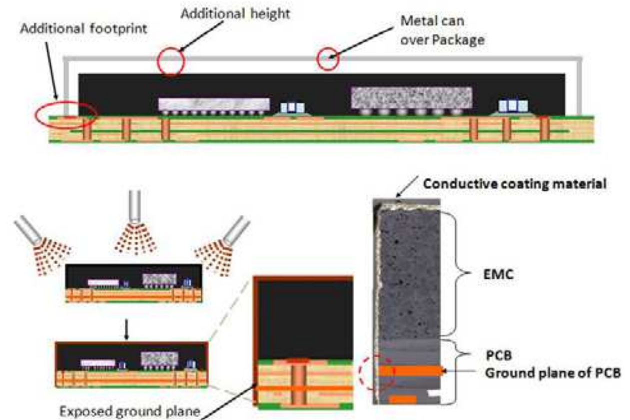


Fig. 19 – Conformal Shielding for RF Application

Other Considerations in System Integration

Design for Manufacturing (DFM) requires the SiP development to fit in the high volume production category, and design rules must be checked carefully when doing the component placement for the SiP design. Design for Testing (DFT) not only must consider testing the overall system functions, but it also needs to add some functional tests for individual components involved in the SiP. A reusable SiP design is also desirable for the system company involved as the SiP can then be applied in its various product lines.

Conclusions

System integration is desirable by a system company in order to meet various market needs with higher performance, smaller package size, and lower overall cost. Compared to SoC solution, system level integration at packaging level may provide benefits that are more cost saving, more flexibility, and possess a shorter development cycle.

System companies must collaborate well with related component companies and the related package companies in order to define an appropriate SiP module. System partitioning is key to identifying a good SiP definition, with an appropriate packaging format be considered carefully. A good balance of considering SiP performance, packaging miniaturization, system overall cost, DFM&DFT, and reusable situations is the objective for system integration.

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