POSSUM™ Die Design as a Low Cost 3D Packaging Alternative

The trend toward 3D system integration in a small form factor has accelerated even more with the introduction of smartphones and tablets.

Integration has focused on (a) reduced form factor in the X, Y, and Z dimensions, (b) more functions combined within a single package, and (c) improved electrical and thermal performance (reduced electrical and parasitic resistance and lower energy consumption). 3D integration must address the device, package and system roadmaps at a cost that promotes a healthy adoption curve. This area of semiconductor packaging is generating a great deal of research and development with high expectations for acceptance once the technology can meet price penetration targets.

3D system integration at the package level can be a more cost effective approach, providing greater design flexibility than at the die level, where multifunctional integration does not necessarily scale equivalently in terms of cost/performance by node. Some of the popular packaging approaches driving 3D integration include Package on Package (PoP), 3D die stacks using wire bonding, and 3D die stacks using Through Silicon Vias (TSV) and flip chip assembly. TSV is one of the most active areas of research and development in semiconductor packaging with significant revenues projected over the next 5-10 years in anticipation of its commercialization. TSV implementation requires considerable commitment in terms of expensive capital investment in equipment and tooling — from wafer handling to stacked assembly and test. Fabrication steps, such as etching through the holes on the back of the wafer, also add significant cost to the final assembly.

To present customers with 3D integration advances at a price that allows them to compete in their target markets today, Amkor has leveraged our expertise with Chip-on-Chip (CoC) and face-to-face device integration to promote the POSSUM™ chip attach methodology. Amkor has spent three years developing and implementing various CoC face-to-face technologies. There is much interest from the microelectronics community because of the modular approach to die integration, the ability to preserve speed and bandwidth without introducing excessive latency or parasitics, and the lower costs involved to produce effective 3D solutions for today’s products.

Face-to-face Chip-on-Chip (CoC) Technology

There are many ways to stack die:

- Face-to-face IC assembly is the joining of two or more dies with their final metal circuitry facing each other. Joining is done through flip chip assembly as opposed to wire bonding.
- CoC assembly where both dies face up in a pyramid configuration (small on top of large) has the top die wire bonded to the bottom die or substrate. The bottom die would also be wire bonded to the substrate.
- CoC assembly where the bottom die faces the substrate and mounted through flip chip attach, has the top die mounted facing up and, again, is wire bonded to the substrate (unless the bottom die contains TSVs).

Customer adoption of all three forms of CoC assembly has been well received. However, in order to get the closest connection between the active circuitry on each die without the expense of introducing TSV processing, the face-to-face configuration is employed. It is being sought in markets as diverse as automotive sensors, logic and memory, MEMS (timers, accelerometers, gyroscopes), optoelectronics and microcontrollers. This is because it uses the existing chip attach or thermocompression (TC) infrastructure and can be ramped to HVM without complex wafer handling processes, making the cost less expensive than TSV approaches. Although it is not a TSV replacement, it enables high performance integration today and will be an adjunct to full TSV integration tomorrow.

The POSSUM™ Assembly Approach

The POSSUM™ stacked die configuration describes two or more devices assembled face-to-face where a smaller die is nested within I/O-free areas of the larger die. The larger of the two dies is referred to as the mother die and the smaller one is called the daughter die. As shown in Figure 1, the daughter die is flip chip mounted onto the face of the mother die so as not to interfere with the mother's surrounding flip chip bump pattern. The POSSUM™ assembly can be mounted onto a substrate as a CSP or BGA. It can also be mounted within a lead frame package or directly onto the PCB as a WLCSP.

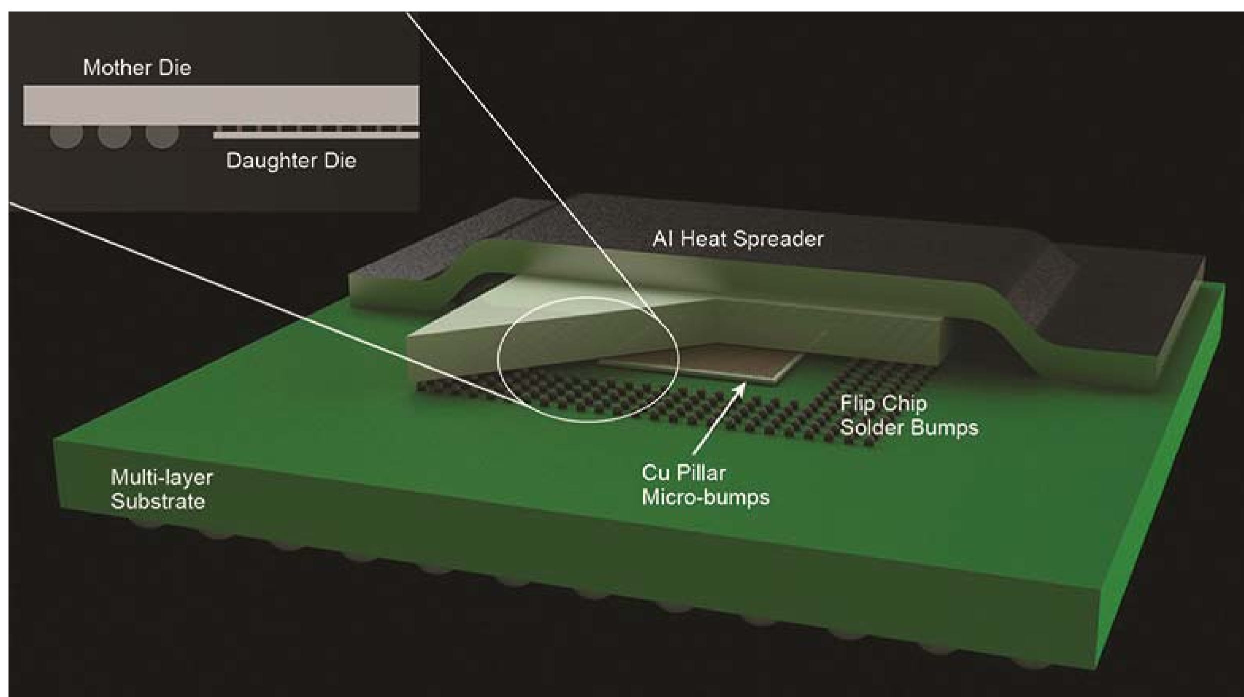


Figure 1. Conceptual illustration of a POSSUM™ assembly where the daughter die is mounted face-to-face with the larger mother die. The mother die is then flip chip mounted onto a substrate or board.

Flip chip face-to-face processes are relatively simple. The flip chip bumps are applied to both mother and daughter dies followed by Wafer Backgrinding (WBG) and dicing. In addition, the mother die can be singulated or can remain in wafer form depending upon the optimized process flow. The daughter die is thinned and joined to the mother die through copper pillar micro-bumps. The combined height of the copper pillar micro-bumps plus the daughter die thickness is designed to be less than the collapsed flip chip bump that surrounds the daughter die. This is to enable sufficient assembly clearance between the daughter die and the next assembly surface. The choice of interconnect technology, whether copper pillar, solder ball or new material interconnect is chosen to accommodate the structural and performance requirements of the stacked multi-die system.

The copper pillar micro-bumps are currently in HVM production at 40µm/80µm staggered pitch and LVM at 30µm/60µm staggered pitch. Two different chip attach assembly processes have been adapted for face-to-face copper pillar bonding:

1. MR-CUF: Mass Reflow with Capillary Underfill has been used for pitch >80µm although this is being extended to 50µm capability. Capillary underfills have filled solder joint gaps between 30µm-50µm on POSSUM™ attached mother and daughter dies.

2. TC+NCP: Thermocompression bonding with Non-Conductive Paste is currently used in HVM production for die with pitch <80µm. Mass reflow has the advantage of self-alignment of the solder bumps during solder reflow while TC+NCP has been found to be a very high yielding and extremely reliable process for finer pitch devices. In addition, thermocompression bonding is a preferred assembly process for devices that may otherwise be compromised by the use of underfills, mold compounds or other material sets that would fill the entire chip-to-chip gap.

Bump technologies that have been developed for the POSSUM™ assembly methodology include conventional copper pillar microbumps and SnAg solder bumps. Other interconnect structures that are being pursued involve chip attach structures chosen to provide for a given combination of standoff, reliability, electrical or thermal properties.

Amkor has tested POSSUM™ assemblies using both similar and dissimilar bump technologies. Examples of similar bumping technologies are plated copper pillar micro-bumps (plated Cu+SnAg cap), plated SnAg solder bumps or pre-formed SnAg solder balls. Packages using Cu+SnAg have passed -55 to 125°C for 2000 temperature cycles (JESD22-A104D, Level B) and packages incorporating dissimilar bump technologies (ex: Ni+SnAg joined to Cu+SnAg bumps) have passed aggressive customer temp cycle testing at -55 to 155°C for 2000 cycles. Examples of interconnect approaches involving dissimilar materials might involve bump structures comprised of non-collapsible core materials to achieve desired spacing and electrical characteristics.

As expected with any new assembly approach, as various stacked constructions are investigated, they are modeled and tested to meet reliability standards. Once feasibility is demonstrated and the structure is characterized and qualified, it is then released to operations to implement a high yielding and production worthy HVM process.

The Double POSSUM™ Approach for Dense 3D Packaging Without TSVs

The chip-on-chip face-to-face POSSUM™ design is very attractive to 3D integration because it provides:

- A close coupling (shorter, faster) communication path between mother and daughter die,
- Less inductance, cross talk and parasitic resistance than wire bonding (providing for high frequency applications and wider bandwidth),
- Improved heat dissipation through an integrated heat spreader (IHS).

Figure 2 illustrates a Double-POSSUM™ package. The Double-POSSUM™ design is actually defined by two levels of nesting die. The daughter die (red) is flip chip attached to the mother die (blue) which is then attached to another silicon die (yellow) instead of a substrate or board. This largest die is then flip chip attached to the substrate or board. The levels of nesting are dependent upon the overall profile of each assembled die, including warpage factors and the inclusion of any added materials such as non-conductive pastes, underfills, mold compounds, etc.

In Figure 2, three daughter dies are copper pillar micro-bumped and assembled onto the mother die. The mother die shows three rows of perimeter pitch solder bumps that are taller than the assembled daughter die to provide sufficient clearance to the next die, substrate or board surface — in this case, the largest (yellow) die that is flip chip attached onto a substrate. This large die then becomes the (grand)mother die of the newly defined structure. Several aspects of this construction are patent pending.

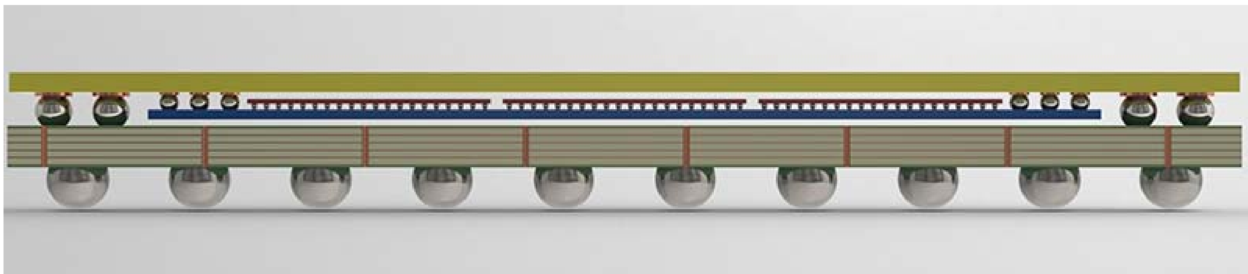


Figure 2. Double POSSUM™ multi-stacked die configurations without the use of TSVs. Multiple die types such as MEMS, ASICs, microcontrollers, memory, etc. can be nested through this method.

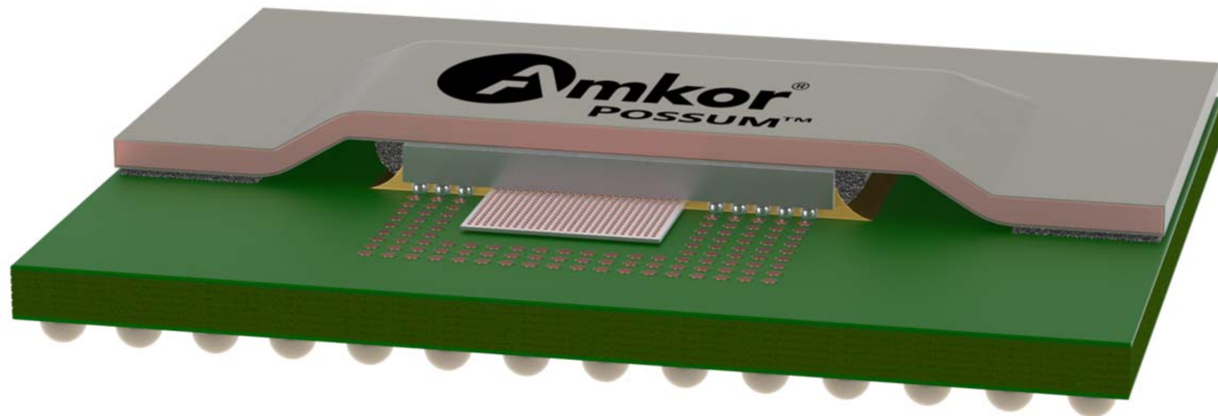
The POSSUM™ assembly as a game changer for MEMS packaging

The Double-POSSUM™ design can be applied to MEMS devices to create 3D integrated systems without relying on the presence of TSVs. Instead, the innovative package design will provide the close die-to-die coupling necessary for the high frequency demands of the system. Current MEMS packaging still uses wire bonding where hybrid capped MEMS and ASICs are assembled side-by-side in a single package. To reduce footprint and preserve signal integrity, variations of the POSSUM™ packaging approach are being considered, including the Double-POSSUM™ design. When working with high frequency oscillators, accelerometers or gyroscopes, roadmaps for MEMS packaging look ahead 5-10 years.

The current use of wire bonds to connect the MEMS device with an ASIC increases cross talk and parasitic resistance. Instead, a MEMS die (or array) can be thinned and flip chipped on top of an ASIC. Copper pillar technology also allows for more I/O connections which means that multiple devices can be can be assembled within a given level of the nested stack. In this example, one or more MEMS die can be assembled onto an ASIC together with memory die, microcontrollers, etc. to realize 3D system integration at the packaging level similar to Figure 2.

Summary

The creation of chip-on-chip solder joints are exceptionally high yielding processes that also pass high reliability JEDEC testing. They provide the foundation for innovative 3D packaging approaches such as the POSSUM™ face-to-face, low profile stack or more complex nested POSSUM™ assemblies. Face-to-face bonding, whether incorporated into die-to-die or die-to-wafer process flows, extends system design options. The POSSUM™ assembly technology changes the thinking surrounding functional integration tactics. Tradeoffs between SoC and SiP approaches from a total cost of ownership perspective have long term and profound roadmap implications. The POSSUM™ packaging approach offers an alternate form of high speed, high signal integrity, die-to-die communication that does not need to be supported through a silicon interposer or TSVs. The technology is expected to compliment and extend TSV packaging approaches in the future while providing for a less costly interconnection methodology for nearer term requirements.



About Amkor Technology

Amkor Technology, Inc. is one of the world's largest providers of advanced semiconductor assembly & test services. Founded in 1968, Amkor has become a strategic manufacturing partner for hundreds of the world's leading semiconductor companies and electronics OEMs, providing a broad range of advanced package design, assembly and test solutions. Amkor's operational base encompasses more than 5 million square feet of manufacturing facilities, product development centers, and sales & support offices in Asia, Europe and the United States. Amkor offers a suite of services, including package design and development, wafer probe and package test, wafer bumping and redistribution services, assembly and final test.