Embedded Die Packaging Technologies Enable Innovative 2D and 3D Structures for Portable Applications

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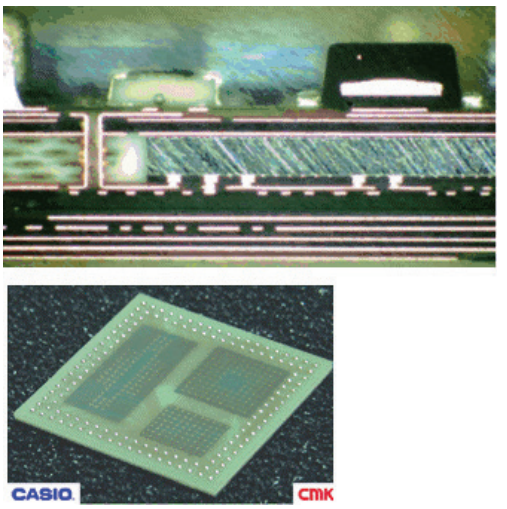
Modularization has become a critical focus throughout the semiconductor industry resulting in sophisticated packaging approaches to address the desire for miniaturization and increased levels of integration. At the lower end, the long standing incumbent technology that has customarily addressed this, Multichip Modules (MCM), leverages traditional multichip attach methods using standard and advanced organic substrates. At the highest end, the most advanced technology platform (2.5D TSV) leverages silicon interposers with metal vias to provide a highly integrated version of the incumbent, but at a cost premium. In the middle, the Embedded Die platform provides perhaps the most compelling argument, especially from the mobile perspective. The embedded die platform cuts a clear path between each of the previous two technology platforms mentioned. The embedded die platform provides opportunity for true System-in-Package (SiP) architectures with much higher levels of integration than the incumbent MCM at much lower costs than the 2.5D TSV platform.

The combination of increased I/O density, reduced footprint, and multi-die capability within a single platform makes embedded die an attractive solution. Additionally, embedded die products offer flexible memory configurations with routing above and below the die in addition to standard JEDEC pin-outs, while also providing integration of disparate die technologies onto a single platform. Thus, a new era of innovation has resulted with increased die content and functionality moving to the packaging industry to address the resulting integration gap. Embedded die is a key enabling package technology that addresses many of these roadmap requirements.

EMBEDDED DIE EVOLUTION

The term Embedded Die is defined as a passive component or an integrated circuit that is placed or formed on an inner layer of an organic circuit board, module, or chip package, such that it is buried inside the completed structure, rather than on the top or bottom[1]. An example of an embedded die module is shown in Figure 1. The benefits of embedding active die include miniaturization, improved electrical & thermal performance, heterogeneous integration, opportunity for cost reduction, and streamlined logistics for OEMs.

Figure 1: Embedded Die Structure (courtesy of Casio/CMK)



Embedded die technologies have been in existence for many years. Passive components, such as decoupling capacitors, are routinely embedded in laminate substrates. Embedded decoupling takes advantage of the capacitance between the power and ground planes in a printed circuit board to suppress the switching noise of high speed digital packages. Embedded active die, though not as common, has seen a resurgence due to improved technology, higher yield, and increased demand for heterogeneous integration in the semiconductor industry. Examples of embedded active die include Fan-Out Wafer Level Packaging (FO-WLP), such as Freescale's Redistributed Chip Package (RCP) and Infineon's Embedded Wafer Level Ball Grid Array (eWLB). Another popular medium for embedding active die is within a laminate circuit board. Laminate embedding technologies include Imbera's Integrated Module Board (IMB) and AT&S' Embedded Components Packaging (ECP®). In addition, several research projects and consortiums have addressed many of the technical and supply chain challenges associated with embedding active die, including the European Hiding Die project, HERMES, and the Casio & CMK EWLP consortium, with a common goal to develop a cost effective die embedding technology

to the maturity level that is ready for industrialization.

Traditionally, the act of embedding die has been burdened by factors such as dedicating a known good die to a poor yielding substrate build-up process, long cycle-time, and the difficulty to inspect, test and rework the embedded die structure. Recently, however, companies are making significant advancements to minimize these issues and develop an infrastructure to support the growing demand for embedded die products. Shifting the die embedding to mid-stream in the circuit build-up process helps to reduce die yield loss. In addition, leveraging mature, large format thin film build-up and substrate lamination processes, in conjunction with high throughput die attach and panel-based assembly equipment helps to ensure a more robust and efficient process. As a result, this has created a market shift towards the increased use of embedded die for 2D and 3D applications.

MARKET SHIFT

Planar scaling has reached an inflection point and as a result, advanced packaging technologies require higher levels of integration, thinness, and cost effective solutions. Consequently, 3D packaging with embedded die solutions has become more attractive as an integration tool for next-generation devices.

Traditional multichip attach methods using standard and advanced organic substrates are limited to 2D planar scaling for MCM applications. The most advanced technology platform (2.5D TSV) is burdened by high packaging cost and an immature supply chain. Embedded die provides an alternate path for true heterogeneous integration in a 3D architecture within a cost structure that is attractive for consumer applications. In fact, both integrated device manufacturers and fabless companies are projecting significant growth for embedded die products, primarily for mobile applications. Figure 2 shows the embedded active market forecast as projected by TechSearch International.

Figure 2: Embedded Active Market Forecast (million units per year)

Product	2012	2013	2014	2015	2016	2017
Power management modules	0.5	7	10	15	75	90
Power modules (voltage regulators)	110	120	180	240	280	300
Automotive	0.005	0.2	40	57	60	70
FO-WLP *	616	702	869	1,043	1,276	1,517
RF modules/boards	1	2	10	60	130	220
Application processor for PoP (laminate process)	-	-	80	185	213	245
Medical (hearing aids)	-	-	0.45	2.66	2.7	2.8
Total	727.5	831.2	1,189.5	1,602.7	2,036.7	2,444.8

Source: TechSearch International, Inc.

**Note: FO-WLP above is comprised of baseband, RF, and power management ICs (which are predominantly 2D structures)*

EMBEDDED DIE PLATFORMS

Current embedded package formats are almost as diverse as the applications themselves, driven not only by manufacturing methods, but also by the system design and strategy to maximize gains from modularization.

Embedding Passives for Noise Reduction

One example of embedded die technology allows capacitive component placement within the substrate. Capacitor placement near the processor is an effective step in the art of noise reduction. Surface mounted capacitors, however, are typically placed as far as 3mm away from the die to abide by capillary underfill design rules. On the other hand, an embedded capacitor can be placed just below the die, reducing the inductance path while freeing up valuable surface real estate at the same time.

Active Device Embedding

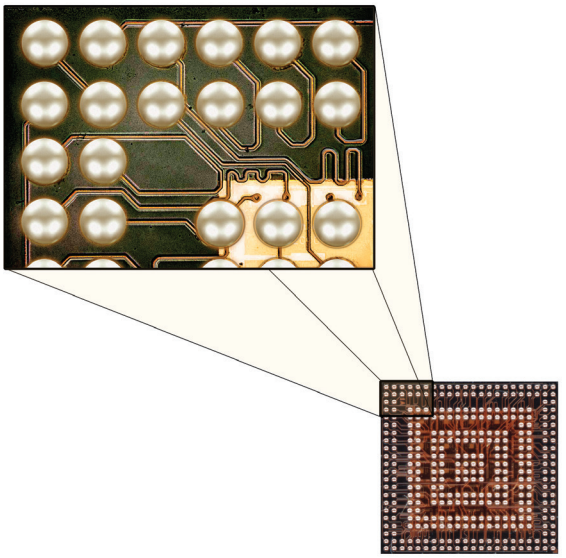
Usually, an active die is embedded to reduce package height. There are a number of ways to embed die, but the final package format generally falls into one of three categories:

1. Fan-Out Wafer Level Packaging (FO-WLP)
2. Embedded Die in Laminate
3. Modular Embedded Die

1. FO-WLP

With FO-WLP processing, the first process step is to place a singulated die on a wafer carrier. This process sequence is known as the "Die-First" process. After the die is placed, the package infrastructure is then built-up around the die to create a reconstitute molded wafer. The advantage of placing the die first is that the die attach reflow step is skipped, since the fan-out circuit is grown directly onto the die bond pads. The disadvantage of this process flow is that any yield loss is a de facto loss of good silicon. A FO-WLP package is shown in Figure 3.

Figure 3: Example of a Typical FO-WLP Structure



2. Embedded Die in Laminate

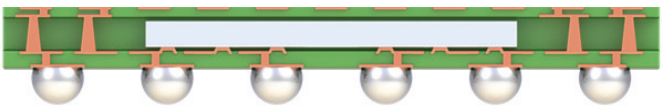
Embedded die in laminate is also a "Die-First" process. It is similar to FO-WLP in that the die is attached first to a carrier, then the package is built up around it. The major difference is that the processing occurs in panel format and the embedding mediums are materials typically used for substrate manufacturing (e.g., resins, dielectrics, build-up materials). ASE's aEASI and J-Devices' WFOP are examples of this technology.

Another approach to embedded die in laminate is to pre-fabricate

See **Portable Applications** *page 18*

the fan-out structure in substrate form then use only known-good units for chip attach. This is known as a "Die-Mid" process flow and the primary benefit is to decrease the cost of yield fall-out. An example of a Die-Mid structure is shown in Figure 4.

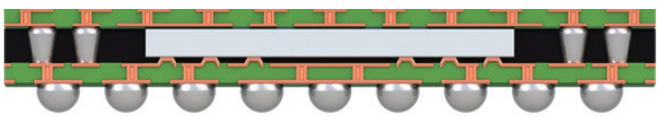
Figure 4: Embedded Die in Laminate (Die-Mid) Structure



3. Modular Embedded Die (Die-Last Process Flow)

The next logical evolution of the "Die-Mid" process is the "Die-Last" process flow, where embedding die takes a more modular approach. In this flow, top and bottom substrates are prefabricated so the die can be embedded as one of the final process steps. The benefit of this method is that it utilizes only known good substrates and minimizes yield loss of known good die. This is particularly advantageous as the embedded die I/O count and substrate complexity increase. Figure 5 illustrates a Modular Embedded Die structure.

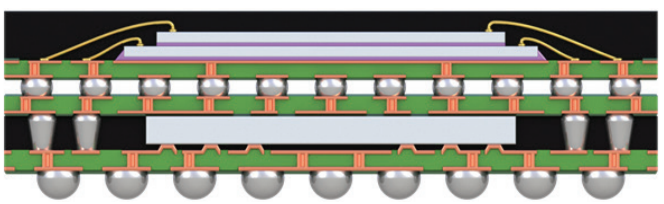
Figure 5: Modular Embedded Die Structure



Package-on-Package

All three of the aforementioned manufacturing methods can support Package on Package (PoP) formats. The major technology enabler for stacking packages is the interface connection from the bottom package to the top package interface, driving the maximum I/O density. The top package interface itself can be either a standard JEDEC PoP or a custom fan-in configuration. An example of a Fan-In PoP is shown in Figure 6.

Figure 6: Fan-In PoP



Form Factor Reduction

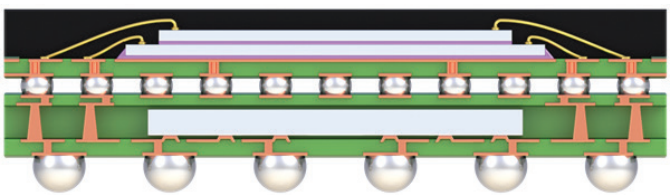
There are several reasons embedding technology can reduce package thickness and overall form factor. **First: Coreless.** Since most embedded fan-out structures use a temporary carrier, a substrate core is not needed. **Second: Layer Reduction.** Shrinking the line and space geometry allows for higher circuit density, which can lead to layer reduction. **Third: Thinner die.** Embedded silicon is better protected from impact damage (e.g., chipping) than if it was surface mounted. Embedded die is also buffered from thermo-mechanical stress by being situated closer to the package's neutral point. Consequently, an embedded package can support thinner die.

True System-in-Package

Embedded die technology is driving true SiP architectures, enabling more than just a typical multi-chip module. The greatest benefit of the SiP architecture is the ability to bring together disparate technologies to create a highly integrated system where the cost, size, and performance are fully optimized. This is made possible by integration with reduced circuit length, improved dimensional tolerances, and enhanced noise reduction to produce a higher performing product. However, higher levels of system integration demand a comprehensive system design strategy as well, which requires early cooperation amongst all parties along the value-add chain, especially the assembly provider.

For OSATs, higher levels of system integration result in more package configurations, which drive the need for flexibility, cost containment, and higher assembly yields. To manage this balance one solution is to embed die at the panel level in a "Die-Mid" process flow. Amkor Technology is currently developing this approach, incorporating an embedding die process using state of the art substrate technology to allow circuit customization for maximum flexibility with high yield potential. This embedded die in laminate structure provides a top-side interconnect, allowing a true System-in-Package heterogeneous architecture. A typical application demonstrating integration of an embedded logic IC with a memory package is illustrated in Figure 7

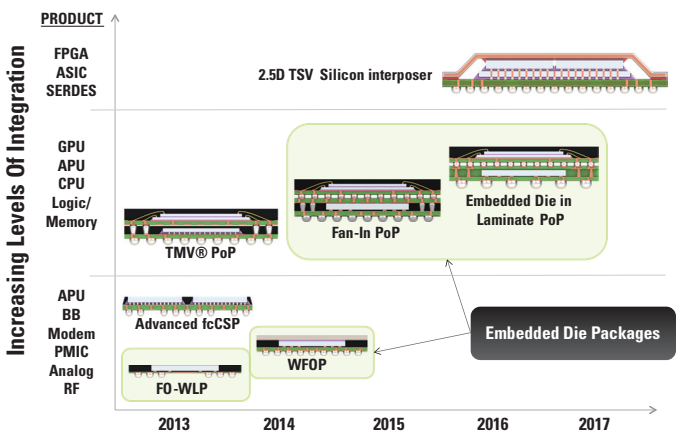
Figure 7: Embedded Die in Laminate PoP (with Logic and Stacked Memory ICs)



LONG-TERM ROADMAP

The semiconductor industry continues to place increased demands on IC packaging technology for advanced portable applications. Heterogeneous integration is driving the need for thin, cost effective, and scalable packaging techniques. Figure 8 illustrates how embedded die technology is meeting the needs of these roadmap requirements.

Figure 8: Advanced Package Integration Roadmap



As shown in the bottom section, FO-WLP and WFOP embedded die technologies are best suited for 2D applications (both single die and MCM structures). Examples include application processors, baseband processors, power management ICs, and combo chips. These devices can typically be supported with one or two layers of conductive build-up circuitry which is optimum for these 2D embedding techniques (from a cost and reliability standpoint).

As illustrated in the middle section, laminate-based embedded die

See **Portable Applications** *page 19*

technology is best suited to support 3D PoP applications, such as Logic + Memory integrated structures. Fan-In PoP and Embedded Die in Laminate PoP benefit from their inherent ability to provide a high density interconnect pattern on the top of the embedded die structure to mount a separate package using traditional SMT techniques. A common PoP configuration is to embed an application processor in the bottom package and mount a memory package on top, which provides a streamlined logistic flow for multi-sourced memory devices.

And finally, the top section shows that 2.5D TSV technology, which leverages silicon interposers with metal vias, is targeted for high-end products, such as FPGAs, ASICs, and memory devices that require very high I/O and interconnect densities. Although 2.5D TSV comes at a cost increase, it allows for higher levels of integration that are not possible with embedded die in organic substrates.

CONCLUSION

The dramatic growth in the portable handset, tablet, and networking markets has been fueled by consumer demand for increased mobility, functionality, and ease of use. This, in turn, has been driving an increase in functional convergence and integration of IC devices, resulting in the need for more complex and sophisticated packaging techniques. Traditionally, multichip modules have enabled heterogeneous integration, but MCMs are limited to 2D planar scalability. 2.5D silicon interposers provide very high levels of integration in all three dimensions, but its cost structure and supply chain have not yet matured to the level needed for commercialization. Embedded die technology bridges the gap between traditional MCM and new advanced 2.5D package solutions, providing increased levels of integration and reduced form factors within a cost structure conducive to consumer applications. Exciting new embedded die structures, such as WFOP, Fan-In PoP, and Laminate Build-up PoP, are poised to meet the modularization requirements for portable communication devices, now and in the future. ■

About the Authors

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References

[1] Carpenter, Karen, Linda Matthew, and E. Jan Varadaman. Embedded Components: Why Now? Market, Applications, and Technologies, Austin: TechSearch International, 2014. Print.