Silicon wafer integrated fan-out technology

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The tremendous growth in the mobile handset, tablet and networking markets is fueled by consumer demand for increased mobility, functionality and ease of use. This increased demand, in turn, is driving an increase in functional convergence and 3D integration of IC devices, which require more complex and sophisticated packaging techniques. A variety of advanced IC interconnect technologies, including through-silicon via (TSV), chip-on-chip (CoC) and package-on-package (PoP), are addressing this growing need. In particular, emerging wafer-level fan-out (WLFO) technologies provide unique and innovative extensions into the 3D packaging arena.

As a platform, WLFO is designed to provide increased I/O density within a reduced footprint and profile for low-density, single- and multi-die applications at a lower cost. The improved design capability of WLFO is due, in part, to the fine feature characteristics associated with wafer-level packaging (WLP). This capability allows for the application of more aggressive design rules, compared with competing laminate-based technologies. In addition, the unique characteristics of WLFO enable the creation of innovative 3D structures that address the need for IC integration in emerging mobile and networking applications.

Design rules and 3D integration capabilities of traditional WLFO technologies, however, are limited by processes and equipment used for circuit patterning. For the most aggressive designs, TSV processes must be incorporated, which often exceeds the cost budget and design requirements needed for the device. Consequently, there is a gap between the design capabilities of WLFO and TSV that needs to be addressed.

Figure 1 illustrates the gap for advanced fan-out applications where disparate die integration is needed on a single platform. To close this gap, Amkor has developed Silicon Wafer Integrated

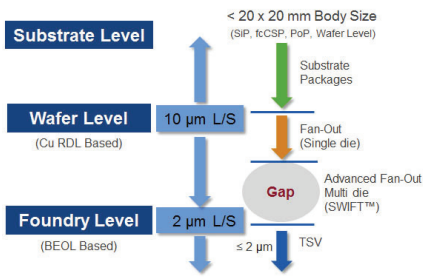


Figure 1: IC package technology integration roadmap.

Fan-out Technology (SWIFT™) as an extension to the fan-out platform. SWIFT incorporates conventional WLFO processes with leading-edge thin-film patterning techniques to bridge the gap between TSV and traditional WLFO packages.

Conventional wafer fan-out technologies

To appreciate the advantages of this technology extension, it is first important to understand the general process flow for conventional 2D and 3D WLFO packages and the limitations of these platforms, as they exist today.

2D wafer-level fan-out. The fundamental WLFO technology is a 2D configuration, based on embedding die into a molded wafer, also called "wafer reconstitution." The molded wafer is processed through a standard WLP flow to create the final IC assembly structure. The active surface of the die is coplanar with the mold compound, allowing for the "fan-out" of conductive copper traces and solder ball pads into the molded area using conventional redistribution layer (RDL) processing [1].

By eliminating the conventional laminate substrate, and opting instead to leverage WLPs superior design and feature size capabilities, WLFO provides many benefits, including: 1) Increased I/O density; 2) Reduced form factor (including z-height); 3) Improved electrical and mechanical performance; 4) Multi-chip capability; 5) Outstanding cost/performance capability (through co-design optimization); 6) Scalability within a heterogeneous assembly platform; and 7) Opportunity for advanced 3D structures.

Two-dimensional (2D) WLFO is well-documented as a robust and reliable WLP technology for electronic devices. **Figure 2** illustrates a cross section of a typical 2D WLFO structure.

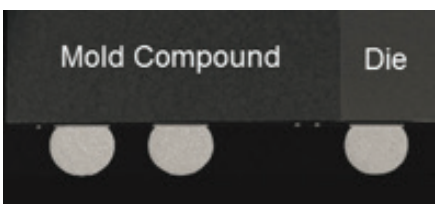


Figure 2: WLFO cross-section.

3D wafer-level fan-out. Standard WLFO technology can be expanded in the vertical (z) direction when connecting it as a 3D PoP structure, as shown in **Figure 3**. This is a common packaging

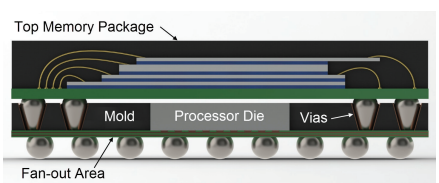


Figure 3: 3D WLFO PoP package structure.

technique used in mobile products to integrate application processors and memory devices [2]. Advanced laser and via fill processes enable the creation of 3D PoP WLFO structures.

The front side (i.e., active die side) RDL process for 3D PoP WLFO is nearly the same as standard 2D WLFO. However, a laser drilling (or equivalent) process is used to expose an RDL feature from the back side (i.e., the mold side) of the package to create through-mold via (TMV®) interconnects. **Figure 4** illustrates the key process steps for the 3D PoP WLFO fabrication process.

Although the 3D PoP WLFO structure looks very similar to a conventional

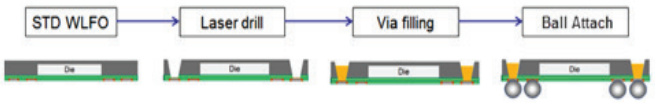


Figure 4: 3D WLFO key process steps.

Figure 5: Comparison of 3D/PoP package structure: a) WLFO type, and b) PCB type.

laminate-based TMV PoP (as shown in Figure 5), 3D PoP WLFO has additional technical merits due to WLP technology. For example, the WLP process uses much thinner conductive and dielectric layers compared with typical laminate substrate build-up technology. The resulting WLFO RDL stack-up has fewer parasitic elements, which provides improved electrical performance. In addition, eliminating wire bonds or flip-chip bumps provides the opportunity for cost reduction. And finally, the ability to thin WLFO packages while still in wafer form creates very thin package structures for PoP applications.

Limitations of standard WLFO technologies

Limited line and space capabilities for the RDL fan-out structure are a key restriction of traditional WLFO. Typically, mask aligners image the photoresist and dielectric materials for WLFO packages. Because of mask aligners' limited depth-of-field, this patterning technique is highly dependent upon the topology of the surface to be developed. Planarizing spun-on liquid dielectrics and photoresists can be very difficult to control on a molded reconstituted wafer, especially when multiple layers of RDL are required. The surface topology is also affected by the inherent warpage associated with molded wafers. Consequently, it is very difficult to achieve fine resolution features of <10/10µm line/space on WLFO.

Additionally, it is difficult to create 3D structures for PoP and other 3D interconnect structures using conventional WLFO technology. The difficulty is due to the challenges of inserting or forming vertical connections within the molded wafer. Because the fan-out copper RDL is created post-mold, complicated laser drilling and copper plating techniques must be applied to the back side of the molded wafer to form 3D interconnects from the front-side RDL layer. An alternative approach is to mold prefabricated 2-layer substrate inserts within the reconstituted wafer [3]. This technique can, however, add significant cost and process challenges.

final point about traditional WLFO technology is that its overall yield is highly dependent upon the quality of the RDL build-up technology. Unlike traditional wire bond and flip-chip assembly on organic substrates, where die are placed on known-good substrate sites, WLFO die are at the mercy of the inherent defect density of the wafer-level fan-out RDL build-up process. This "die-first" assembly flow requires very high RDL yield to avoid scrapping good die.

SWIFT technology

The new package technology is designed to overcome many of the issues associated with conventional WLFO technology. In addition, it provides increased I/O and circuit density within a reduced footprint and profile for single- and multi-die applications. The new technology's improved design capability is due, in part, to the fine feature capabilities associated with this innovative wafer-level packaging technique. It allows for the application of more aggressive design rules, compared with competing WLFO and laminate-based IC assembly techniques. In addition, the characteristics of the new process enable the creation of 2D and 3D structures that address the need for IC integration in emerging mobile and networking applications.

SWIFT structure and attributes. Figure 6 shows cross-section illustrations of 2D SWIFT and 3D/PoP SWIFT dual-die structures. Although the package appears to be a typical fine-pitch flip-chip construction, it incorporates some unique features not associated with conventional IC packages, including: 1) Polymer-based dielectrics; 2) Multi-die and large-die capability; 3) Large package body capability; 4) Interconnect density down to 2µm line/space (critical for SoC partitioning applications); 5) Cu-pillar die interconnect down to 30µm pitch; and 6) 3D/PoP capability using TMV or tall Cu pillars.

Key assembly technologies enable the creation of these distinctive SWIFT features and attributes. Features of 2/2µm line/space can be achieved using

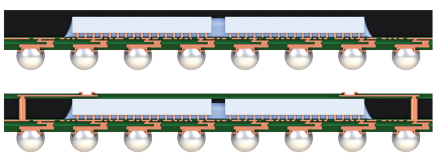
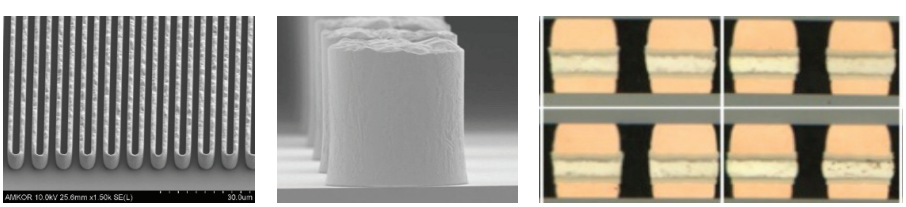


Figure 6: 2D SWIFT and 3D/POP SWIFT dual-die structures.

stepper photo imaging equipment, thereby enabling very high-density die-to-die connections required for SoC partitioning and networking applications where 2.5D TSV would typically be used. Fine-pitch die micro bumps provide a high-density interconnect for advanced products, such as application processors and baseband devices. In addition, tall Cu pillars enable a high-density vertical interface for mounting advanced memory devices on top of the SWIFT structure. These enabling technologies are illustrated in Figure 7.

SWIFT process flow. Attributes of the new technology are realized by applying a process flow that incorporates both flip-chip assembly and wafer-level processing techniques. The process flow is shown in Figure 8.



- Fine L/S RDL > 2µm
- Stepper capability
- Multilayer to 3 layers

- Through mold interface (tall Cu pillar)
- > 100µm pillar height

- Fine pitch micro bump die interconnect
- 30µm pitch capability

Figure 7: Key enabling SWIFT technologies.

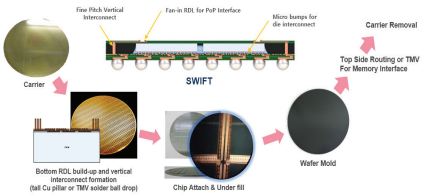


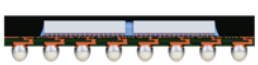
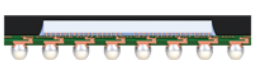
Figure 8: SWIFT process flow.

High-density RDL build-up is performed on a carrier platform using conventional WLP technology. Fine-line and space routing can be applied for high-density interconnect applications. The SWIFT processes' small feature size capability allows for a reduced package footprint. Tall Cu pillars or TMV solder balls form the vertical interconnects. The flip-chip die is attached to the high-density RDL build-up structure and encapsulated with epoxy-based molding compound. Wafer back-grind creates very thin structures. For 3D/PoP constructions, the solder balls are exposed using TMV technology [4]. Or, for fan-in PoP applications, top-side routing is applied using traditional wafer RDL build-up techniques. After carrier removal, solder balls are attached to the BGA pads and the molded wafer is singulated.

SWIFT vs. WLFO technology. Table 1 compares some key attributes of the new process versus traditional WLFO technologies. Although the new approach requires Cu pillar processing at the silicon wafer level, it enables the die to be attached to a pre-inspected known-good RDL structure with very fine-pitch interconnect features. This, in turn, helps ensure known-good die (KGD) are not subjected to any yield loss associated with the RDL build-up process. In comparison, for WLFO, KGD are dedicated prior to RDL creation, which increases the risk for die yield loss because of the inherent defect density of the WLFO process. In addition, traditional WLFO technology requires very high-accuracy die-attach equipment and careful process characterization to minimize the die shift and molded wafer warpage issues that are associated with WLFO processing. Finally, because the SWIFT RDL structure is built upon a flat carrier, the dielectric topology can be controlled to allow fine resolution circuit formation in multiple layers. In comparison, conventional WLFO has limitations on RDL layer count and line/space capability because of the wafer warpage and topology variation intrinsic to molded wafer processing.

Summary

A state-of-the-art fan-out structure, can bridge the gap between TSV and traditional WLFO packages. SWIFT technology is designed to provide increased I/O and circuit density within a reduced footprint and profile for single- and multi-die applications. The distinctive characteristics of this technology are due, in part, to the fine feature capabilities associated with this WLP technique. These capabilities allow for much more aggressive design rules to be applied, as compared with traditional WLFO and laminate-based assemblies. In addition, the new technology enables the creation of advanced 3D structures that address the need for increased IC integration in emerging mobile and networking applications.

Key Attributes	SWIFT	WLFO
Die Wafer processing	Cu Pillar	None required
Die dedication	Die last (on Known good RDL)	Die first
Die attach	High accuracy FC bond on known good RDL site	High accuracy D/A (slow)
Patterning	Photo (stepper)	Photo (mask align or stepper)
Line/ Space	2 - 10um	6 - 10um
# RDL Layers	1 – 3	1 – 2

Table 1: SWIFT vs. WLFO process.

Acknowledgments

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