What is driving advanced packaging platforms development?

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The semiconductor industry is driven by the miniaturization of transistors and scaling CMOS technology to smaller and more advanced technology nodes, while at the same time reducing the cost. To overcome these limitations, new advanced packaging technologies have been developed, enabling more functionality to be integrated along with various types of devices in the same package. A significant level of activity is currently underway within the advanced packaging industry. Research, development, innovation, industrialization and mass market are the advanced packaging industry's key words. The spotlight is shifting towards advanced packaging. This article details the status of advanced packages and reviews some of the most innovative ones.

Which packaging platforms will take the lead?

While technology nodes continue to be developed and innovative solutions are being proposed, the investments required to bring such technologies to production are increasing significantly. The advanced packaging industry is doing well, with solid growth expected and a market value reaching US$30 billion by 2020. Overall, the main advanced packaging market is the mobile sector, with end products such as smartphones and tablets. Other high-volume applications include servers, PCs, game stations, external HDD/USBs, and more [1].

At Yole Développement (Yole), we observed several different packaging approaches available on the market. These solutions clearly depend on the final product and application needs that are of great interest to the industry today. These advanced packaging technologies have increased in complexity over the years, transitioning from single to multi-die packaging, enabled by 3-dimensional integration. They include system-in-package (SiP), wafer-level packaging (WLP) (such as fan-in and fan-out, flip-chip technologies), 2.5D/3D technologies, and embedded dies.

Which packaging platforms will take the lead or garner more interest from the industry? This is the big question that all advanced packaging companies would like to answer.

At Yole, we continue to see a very dynamic ecosystem, a lot of valuable companies and great interest in all of these innovative platforms. Because of the growth of the consumer market, as well as the need for higher performance products (i.e., 4K gaming, networking) both packaging platforms, fan-out and 2.5D/3D TSV, are being used for these applications. Below we provide an overview of the status of these two current package types.

Fan-out packages. Fan-out is in the spotlight since TSMC, the Taiwanese foundry leader, will be producing this type of package for the application processor of the Apple smartphone. Fan-out technology works by embedding a die into a molding compound and redistributing the I/Os to the outside of the die. Initially, this technology was adopted by STATS ChipPAC and NANIUM S.A. with their own proprietary solutions. With the entrance of players such as ASE, SPIL, Amkor Technology and Deca Technologies, and much more, the competitive landscape of this market is intensifying—each player brings different techniques and integration schemes to the table. The advantages and challenges are different for each approach. These include warpage concerns, die shift, and issues with increasing yield and I/O counts, all of which are especially difficult for higher-end, complex applications.

TSMC's preparation for mass production, with its own technology called InFO, will increase the pressure; according to Yole, the market was initially estimated to reach only US$174 million, prior to TSMC's adoption of the fan-out platform [2]. Today, the fan-out market is expected to have the highest growth of all, exceeding US$2 billion by 2020, all platforms included (**Figure 1**). Fan-out technology will not only bring value to several players; the innovative approach could also significantly impact the substrate and flip-chip markets and become a disruptive technology within the entire advanced packaging market. The strategic choice made by TSMC confirms this revolution. It will be very exciting to follow up on the advanced packaging industry landscape to see how the market evolves and see which players will be part of the new ecosystem.

So, is it possible to predict what 2016 will be like? Of course, 2016 will

Figure 1: FOWLP activity market forecast with Apple entry. SOURCE: [2]

see much broader fan-out usage and therefore more investment in equipment to address that demand, including outsourced semiconductor assembly and test (OSAT) companies, integrated device manufacturers (IDMs) and foundries. The complete advanced packaging supply chain is now getting ready to ramp up production to larger volumes.

2.5D/3D with TSVs. Another emerging advanced packaging platform is 3D integration. This solution allows devices to be stacked vertically using through-silicon vias (TSVs) and interconnects for both mechanical and electrical connections. The two major architectures using 3D integration with TSV technology are 2.5D and 3D IC. 3D integration can enable higher memory bandwidth, lower power consumption, and reduced form factor and cost, compared with traditional packaging technologies.

TSV technology was first adopted in production for CMOS image sensors (CIS) and microelectromechanical systems (MEMS) markets and was used for several years. CIS devices continue to be the main application using 3D stacking and TSVs. New sensors such as the ambient light sensor (ALS) and fingerprint sensor have also adopted these technologies. Such technology is not limited to CMOS scaling in itself; rather, it adds functionality by stacking different types of devices, such as X-PUs, together with memory stacks. For the memory segment, the main market is for high-performance computers, networking, gaming and servers. This functional diversification is known as the More-than-Moore concept.

One of the latest products, such as AMD Radeon R9 Fury with its 2.5D configuration, high-bandwidth memory (HBM) stacks, and Samsung 3D TSV stacked dynamic random access memory (DRAM) released in 2015, highlight the added-value of 3D integration platforms. AMD's 3D and 2.5D components integrate HBM-based DRAM dies connected with via-middle TSVs and micro-bumps, as well as a GPU stacked onto a silicon interposer, that also incorporates via-middle TSVs. The graphics market is driven by the need for high performance. The HBM component delivers 60% more memory bandwidth and 3x the performance per watt and consumes 94% less PCB area than GDDR5 [3]. Furthermore, Samsung is an active player in this domain and is entering mass production, driven by the need for higher bandwidth performance. Its new DRAM package, named 4GB HBM2, features 256Gbps of bandwidth, doubling the current HBM1 DRAM package. This year, Samsung is also planning to produce an 8GB HBM2 DRAM package; this second DRAM generation clearly paves the way for wider adoption of 3D TSV stacked memories in lower-end applications within the next three years. As volumes go up and price goes down, Yole's analysts are expecting more announcements from Samsung of course, and also its main competitors [4].

Market status of the 3D integration platform

MEMS and CIS markets are expected to exhibit continuous growth over the next several years, fueled by consumer applications such as smartphones, tablets, wearable products,

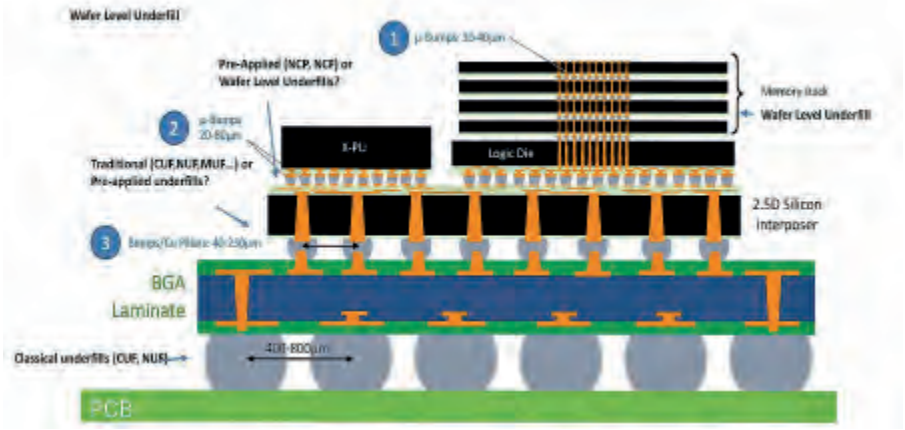

Figure 2: Underfill materials opportunities: flip-chip and 3D packaging solutions. SOURCE: [6]

Figure 3: TB/DB material is mainly used for the 2.5D/3D TSV packaging platforms; from 2015 to 2020 – in M$. SOURCE: [7]

and more. Indeed, the mobile phone industry has grown, producing more than 1.1 billion devices in 2014 [5]. On the high-end market, driven by the need for further performance increases, volatile memory and especially DRAM are clearly opening the doors to the commercial adoption of 2.5D/3D ICs. Original equipment manufacturers (OEMs) are also planning to release products using memory stacks around 2016-2017. These companies are targeting networking applications, routers and switches.

A large range of packaging platforms is available today. All are expected to continue their growth. Fan-out and 3D IC could stand out with the strongest growth rates: 3D integration is now available on the market across a wide range of devices, especially in the consumer market segment. As for fan-out, it has seen the largest growth and a potential move to panel manufacturing in the future.

On the advanced materials side, a lot of incredible innovations have been developed by advanced packaging players. For example, fan-out and 2.5D/3D platforms require creative materials that will provide the most robust manufacturing processes, as well as the lowest cost and most reliable final packaging products (**Figure 2**). Key materials include the items described below:

Dielectrics for redistribution layers (RDLs). Such materials are mostly polyimide/polybenzoxazole (PI/PBO) based. The key technical requirements in fan-out and 2.5D/3D packaging platforms are a low dielectric constant and low dielectric loss, high thermal stability, low-temperature cure processing, fine geometry patterning, process flexibility (coating, patterning, development), low moisture uptake, robust mechanical properties and chemical stability, tunable viscoelastic properties for planarization and gap filling, and high reliability.

Temporary bonding and debonding (TB/DB) materials for further thinning and handling of thin wafers. TB/DB is one such key to technology for handling and double-sided processing of extremely thin TSV wafers for 2.5D/3D platforms [7]. The requirements of temporary bonding materials are numerous. First, they must be compatible with a vacuum process. They must also be stable up to 200°C in order to resist the plasma-enhanced chemical vapor deposition (PECVD) process at 200°C and bump reflow at 260°C. The bonding temperature must be lower than the reflow temperature.

TB/DB materials must also be chemically compatible, meaning they must be resistant to chemicals used during the processing steps, such as chemical mechanical polishing (CMP), and be easy to clean and debond without chemical and thermal stresses. Additionally, such advanced materials must have superior mechanical properties to withstand the wafer thinning process and provide strength to hold the temporary carrier-to-device wafer during high-temperature process steps.

TB/DB materials can be developed using different chemical processes: Brewer Science, JSR Micro, and Dupont focus their materials development on a thermoplastic approach. Thin Materials/Nissan Chemical Industries and Dow propose TB/DB materials using thermosetting technology, while materials from 3M and TOK are part of the photoset type. Shin Etsu, meanwhile, has developed a specific combination of thermoplastic and thermoset composites.

Currently, TB/DB material is mainly used for 2.5D/3D TSV packaging platforms. Related markets are not as significant. At Yole, we estimate these markets to have reached about US$6.3 million in 2015. A 25% CAGR is expected between 2015 and 2020, allowing the market to reach about US$19 million in 2020 (**Figure 3**) [7].

Fan-out platforms could be another potential application, especially when the thickness of reconstituted wafers falls below 400µm. Certain OSATs are currently studying the feasibility of such technology.

Wafer-level underfills (NCP/NCF). NCP/NCF for smaller pitches are one of the key materials used in 2.5D/3D packaging platforms. Capillary underfill (CUF) is probably the most mature and widely used underfill technology. Underfill technology is mainly suited to large interconnection pitches and die-to-die gaps (up to 50µm). In advanced packaging applications (e.g., 2.5D and 3D), the technical challenges are numerous. At Yole, we have identified some of these as high interconnect density, adequate bonding pitch, small die-to-die/substrate gap size, and CUF application. Some of the issues include the cleaning of flux residue, voiding due to difficulty in filling the narrow gap, and longer underfilling times. To overcome these challenges, in CUF applications for example, alternative underfill methods, such as NCP and NCF, have been developed. NCP is better for Cu pillar-thermocompression bonding (TCB) applications, whereas NCF is mainly used for TSV memory dies. The market for NCF is currently small but expected to reach about US$13 million by 2020.

Molding compound is one of the most critical materials in the fan-out platform. It can have a significant impact on performance, cost and reliability in the fan-out advanced package. Such materials are produced by industrial players in various forms, including liquid, granular and film/sheet. Almost all of the fan-out market currently uses a liquid mold compound. Key suppliers are Nagase

ChemX, Hitachi Chemical, and Panasonic. Materials suppliers are also promoting other options, such as granular and film forms, with different characteristics in terms of cost, thickness control and compatibility with panel formats.

Emerging packages and materials aim to bridge the gap by reviving the cost and performance curve while adding more and more functionality. 3D technology and fan-out WLP combined with innovative materials are undeniably part of these new package types as previously described.

The added value of SiP

In parallel with the efforts noted above, another type of architecture has also shown added-value in the advanced packaging industry: the system-in-package (SiP). Particularly driven by the Internet of Things (IoT), SiP is a high-interest packaging approach, as it enables the integration of heterogeneous technology (separating ICs with functional blocks) and reduces cost and form. According to Yole's analysis, the market drivers are numerous and comprise the mobile market, including smartphones and tablet applications, radio-frequency (RF) applications and connectivity modules.

Within the context of the above, industrial players are more and more looking for disruptive platforms and therefore pushing the limits of innovation. The SiP advanced packaging platform could be an answer as well. Indeed, substantial effort has been made at the substrate level, especially with coreless SiP penetration. Latest high/mid-band filters, TQF6405 from Qorvo and AFEM8030 from Avago Technologies, both embedded in iPhone 6s™, point up the added-value of SiP technologies [8,9].

Keys to advanced packaging: miniaturization and modularization

The trends for miniaturization and modularization continue to cause disruption at the system level. The drive for modularization pushes both the foundry (at one end) and electronic manufacturing service (EMS) providers (at the other) to offer services beyond their core capabilities. With advanced silicon nodes continuing to increase in cost, packaging has emerged as a key competitive differentiator—necessitating consideration earlier in the design process.

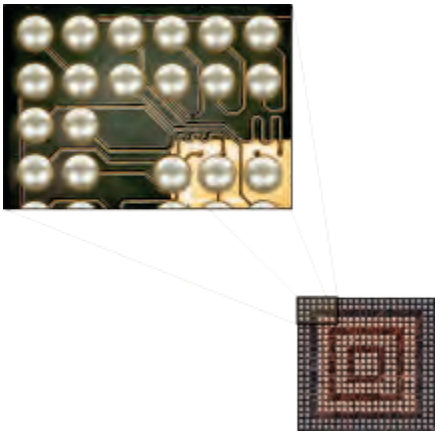

Figure 4: Amkor Technology WLFO.

Figure 5: Amkor Technology Avatar TSV progress.

Advanced packages such as fan-out (**Figure 4**) and those implementing through-silicon vias (TSVs) (**Figure 5**) have become key packaging platforms that effectively address the more recent trends noted above. These two types of advanced packaging technologies provide the modularization and integration required to enable higher levels of system-level performance, delivering higher bandwidth and affording more efficient power management. The use of these latest platform technologies can be found in new

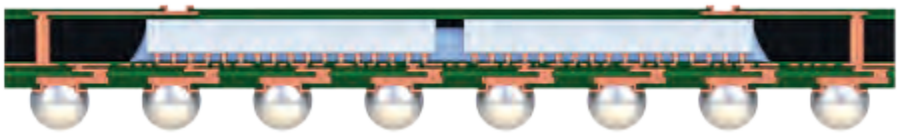

Figure 6: Amkor Technology SWIFT™ top RDL.

Figure 7: Amkor Technology SLIM™ cross section.

product releases spanning the mobile arena to high-end networking, as well as processing. To enable all these newer technologies, closer collaboration between the packaging houses and their customers, as well as additional end-to-end support is essential, including electrical design, characterization and testing. Only the most advanced assembly houses have adequate funding and are able to make these investments. That said, for the leading OSATS, the investment has been made and is now paying dividends with the release and designed-in use of both of these packaging technologies. As a result, advanced packaging is clearly one of the key enablers for the next-generation of sophisticated electronic devices, simultaneously enabling miniaturization and performance optimization.

An example is in SiP technology, which requires the ability to handle multiple process technologies and die for the different functional blocks (analog, mixed-signal, digital), thereby increasing the requirement for state-of-the-art packaging solutions. Fan-out wafer-level package technologies, even at the rudimentary level, enable the most complex SiP solutions, such as mobile RF front-end or MEMS technologies. In addition, by utilizing a yield-conscious "die-last" technology approach (**Figure 6**), package technologies now found in advanced wafer-level fan-out packages such as silicon wafer integrated fan-out technology (SWIFT™), allow for the integration of even higher value die by reducing the risk of die loss due to packaging yield issues typically found in the traditional fan-out approaches. The more sophisticated dies-last approach enables the use of very fine-line lithography down to 2µm line/space and multi-die integration by virtue of a process flow that isolates the high-value die from the difficulty in routing multiple layers at these very fine trace pitches. Ultimately, the dies-last approach removes the crippling effects of losing die due to the intimate tie to fine-line lithography yield loss in the dies-first approach, providing a package technology that is unmatched in value. An example of a package utilizing the dies-last configuration is shown in **Figure 7**, where the integration of memory and high-powered processing is illustrated.

TSV technology is now gaining traction in the semiconductor industry, providing the preferred platform for advanced networking devices as well as the most advanced graphic devices. One strategy for TSV today is the partitioning and use of die at the best technology node where the best price and performance exist. This approach helps to keep foundry costs down by making use of system optimization for memory, analog, performance and power management. In this manner, die costs are correctly relegated to the appropriate node, allowing maximum yield and reducing the overall die size. Another strategy is to place HBM onto a silicon interposer very near the processor to reduce the typical parasitics and inductance issues encountered with on-board memory. This technique specifically addresses the growing need for increased memory integration and provides clear downstream benefits in both power and performance, by serving as a replacement for eDRAM/eFlash. This is the primary attraction to 2.5D TSV today, where a side-by-side format is used to allow reduction in both die size and motherboard size (including layer count).

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