Five Industry-Leading Packaging Technologies

IC packages for implementing next-generation devices to support the connected world of the future

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OVER THE PAST FEW YEARS, THERE has been a significant shift from PCs and notebooks to smartphones and tablets as drivers of advanced packaging innovation. In an industry segment that has grown accustomed to a multitude of package options, consolidation could produce "The Big Five" advanced packaging platforms. These include low-cost flip chip, wafer-level chip-scale package (WLCSP), microelectromechanical systems (MEMS), laminate-based advanced system-in-package (SiP) and wafer-based advanced SiP designs. (See Determining the Big Five below.)

Low-Cost Flip Chip

Unlike the other four platforms, flip chip is not a package platform, but an interconnect method that uses bumps instead of wire bonds to connect the various circuits as well as attach the die to a package substrate. In the case of flip chip, connections are formed over the surface of the die area rather than at the package perimeter, as is the case with wire bonds. Flip-chip technology enables several ball grid array package families. Although WLCSP also uses interconnect bumps, the main distinction between a WLCSP and a flip-chip package is that the after the bump process, the WLCSP die is mounted directly on the printed circuit board and does not have a package substrate.

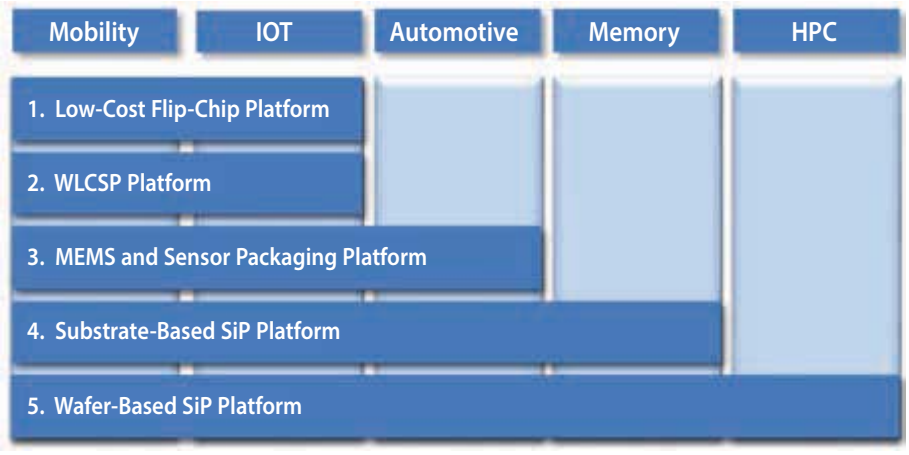
While WLCSP has been the go-to package of choice to meet mobile product requirements, WLCSP reaches a point where it is limited by its die size and the number of I/O it can support. According to Yole Développement, that magic number is roughly 500, typically in an 8 x 8 mm^2 package. Many industry analysts view fan-out wafer-level packaging (FOWLP) as the solution to the increased I/O problem, since it enables higher density by expanding the footprint to slightly larger than the die size - and has lower cost than the flip-chip alternative today. However, emerging low-cost flip-chip solutions will provide more viable alternatives and create the next package platform to pick up where WLCSP leaves off.

Associating "low cost" with "flip chip" may seem like an oxymoron because the early adopters of flip-chip packages were high-performance devices like CPUs, graphical processing units (GPUs) and chipsets. However, as flip-chip processes have matured, the associated costs have been reduced, while still maintaining the performance benefits, making it the ideal platform for other IC technologies such as RF, FPGAs, ASICs, memory, CMOS image sensors, LEDs, and more. In fact, the newest low-cost flip-chip solutions are not only very cost competitive to FOWLP, but they are also competitive in thinness as newer methods are implemented.

Additionally, despite the recent hype regarding FOWLP, it is important to remember that low-cost flip-chip packages are currently dominating the advanced packaging market. Why? Because it's still a better choice than FOWLP for most applications. In fact, FOWLP is cur-

DETERMINING THE BIG FIVE

To zero in on "the Big Five" semiconductor packaging technologies, a team of packaging experts identified five key platforms that they believe will be leveraged across a multitude of applications and markets - both now and in the future. The selected platforms are currently in different stages of adoption and production, and will hold up through generations of development to continue serving the industry needs. The figure shown at right lists the market segments (mobility, Internet of Things (IoT), automotive, high-performance computing (HPC) and memory) and identifies which markets are served by one or more of these platforms.



The Big Five packages target different market segments.

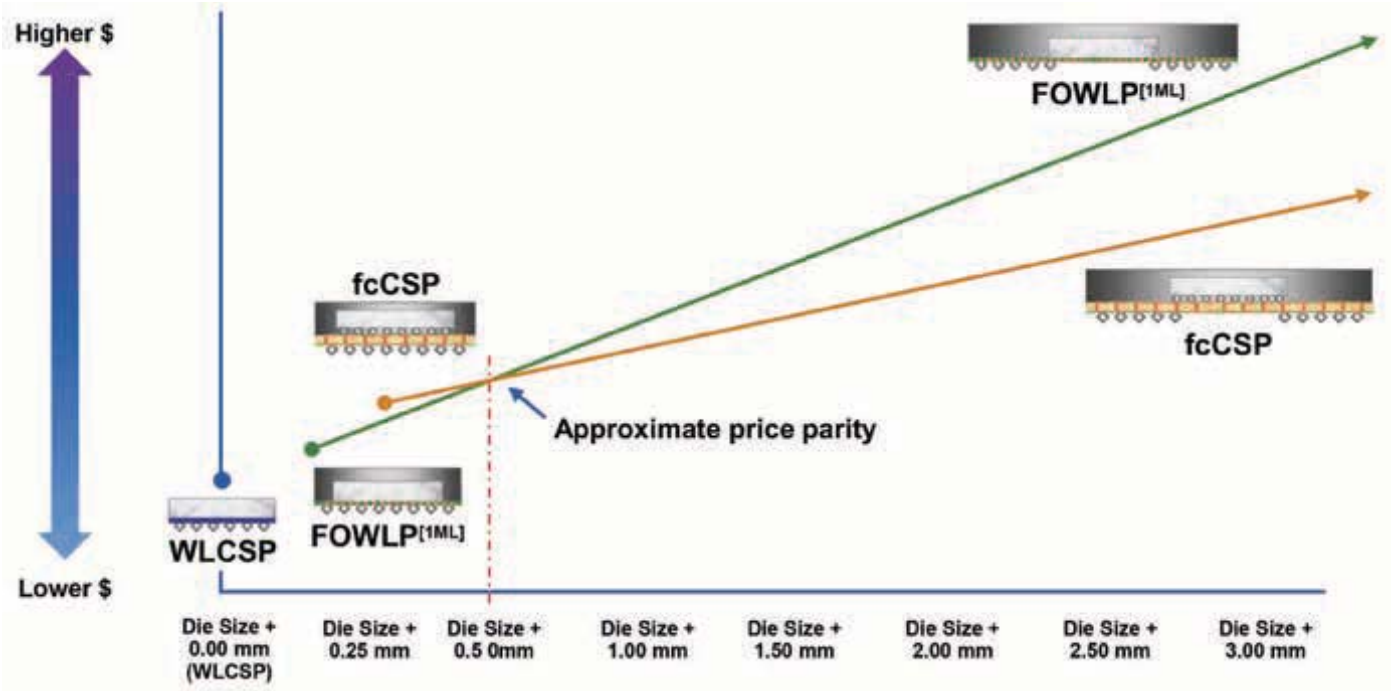


Figure 1. As package to die ratio increases, there is more disparity between the FOWLP and fcCSP.

rently only suited to a small percentage of mobile, wireless, medical and military applications.

While many industry analysts proselytize FOWLPs as a lower-cost alternative to WLCSP than flip-chip CSPs (FCCSPs), FOWLP is lower cost only when the ratio of the package body size to the die size is nearly the same or only slightly larger. Figure 1 illustrates this relationship. The cost of the redistribution layer (RDL) is integral to the overall cost of the package. Standard WLCSP has the lowest-cost RDL impact, although as previously mentioned, its package size is limited to die size only. As the ratio of body size to die size increases, low-cost FCCSP structures become more favorable from a price point perspective. When the package body size is greater than 1 mm more than the die size, the cost for wafer-level redistribution becomes sufficiently high making FCCSP the best path for cost.

As flip chip continues to evolve, it remains more economical and more reliable than most fan-out packages. Investments in low-cost FCCSP technologies have created economies of scale and are driving down the unit cost. FCCSP's use is expanding beyond the computing, mobile and wireless markets, extending into automotive and medical, as well as the next big wave for low-cost applications: the wearable device market for the IoT.

WLCSP: The Workhorse of Advanced Packaging Technology

A WLCSP is a single-die package, limited by the die size, which includes wafer bumping (with or without pad layer redistribution), wafer-level final test, device singulation and packing in tape and reel to support a full turnkey solution.

Now in volume production, WLCSP is the workhorse of the Big Five advanced packaging technologies due to its cost/performance ratio resulting from the elimination of the package substrate. Packaging considerations start with WLCSP, and only move to other formats when routing requirements exhaust the available real estate. Ultimately, customers will choose WLCSP over the other package options where technologically possible because it is the lowest-cost package.

Also known as fan-in wafer-level packaging (FIWLP) industry-wide, WLCSPs are applicable to a wide range of markets and are generally related to analog and mixed-signal, wireless connectivity and automotive device categories. Typical applications include integrated passive devices, codec, power amplifiers, IC drivers, RF transceivers, wireless local area network chips, GPS and automotive radar. WLCSP offers the lowest total cost of ownership, enabling higher semiconductor content while leveraging the smallest form factor. It is one of the highest-performing, most reliable semiconductor package platforms on the market today. From a market perspective, WLCSP is ideally suited for, but not limited to, mobile phones, tablets, netbook PCs, disk drives, digital still and video cameras, navigation devices, game controllers, other portable/remote products and some automotive end applications.

Perpetual innovation is intrinsic to packaging success and focuses on driving existing technologies to lower cost points. With the anticipated growth in the WLCSP market, there are many reasons for improving and optimizing the WLCSP manufacturing process. A good example of optimization is the implementation of die sidewall protection. Although most WLCSPs are not molded, a method has developed to provide mold-like die surface protection. Using this approach, a molding compound is injected into the saw streets and then the wafer is diced again, creating five- and six-sided molded WLCSPs (see Figures 2a and 2b). This process is currently available, and customers are now designing it into their WLCSP requirements.

Die sidewall protection becomes even more critical as silicon nodes scale beyond 14 nm to 10 nm and 5 nm, where the risk of potential sidewall damage intensifies due to brittle dielectrics, smaller bump pitches and more.

MEMS Packaging

Many leading companies and industry experts predict that the growing trend for smart devices (smart cars, smart cities, smart factories and more) will result in the deployment of a trillion sensors, many of which will use MEMS technology. However, MEMS devices are not standard integrated circuits. Creative wafer fabrication techniques produce Si-based transducers and actuators that respond to or interact with, external or environmental stimulus.

At the onset of MEMS packaging, priority was given to solving the end-market application over cost and package form factor. This created a broad diversity of package form factors, with a different approach for almost every application and end market. As the MEMS market grows and transitions into high-volume production, package and test standardization is needed to offer cost-competitive solutions without sacrificing performance. The requirement to control stress to the MEMS structure while allowing stimulus to go through remains the same. The combination of a standard cavity packaging platform and optimized material sets will ensure a near-stress-free environment that allows the MEMS device to function as it was designed to in the real world.

Amkor's focus is creating a standard cavity package platform that will provide the flexibility to support multiple MEMS applications. It will be customizable on the inside while remaining standard on the outside to maintain maximum compatibility during assembly, final test and surface board mount. The standard MEMS platforms will also allow the use of other packaging techniques like FlipStack® technology, through silicon via (TSV), Cu pillar and die stacking for MEMS sensor fusion and IoT applications. Figure 3 shows examples of these packaging approaches.

Figure 2a. 5-sided molded WLP (CSPnl™ technology).

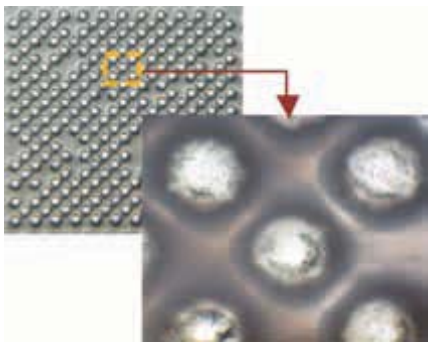


Figure 2b. Top-down view of 5S molded WLP (CSPnl technology).

Sensor fusion, where software combines the data from different sensors to reduce application uncertainty, leverages all types advanced packaging expertise to integrate different MEMS and sensor functionalities with data processing ICs in multi-die packages. FlipStack CSP technology is an example of sensor fusion, where the bottom ASIC die is a flip chip, and the MEMS die is stacked on top and wire-bonded to reduce the overall package footprint.

Advanced MEMS packaging platforms will be essential to achieving the deployment of anything close to a trillion sensors.

Laminate-based Advanced SiP

Traditional laminate-based SiP solutions have existed for some time and have been manufactured by electronic manufacturing services (EMS) providers with printed circuit board (PCB) assembly design rules and relaxed form factors. Advanced laminate-based SiP solutions, on the other hand, are more complex systems that are miniaturized using tighter and smaller outsourced assembly and test (OSAT)-based assembly capabilities. Advanced laminate-based SIP solutions serve a higher end of the market. This is the case for 4G/LTE RF front end modules (FEMs) which require the complex integration of filters, mixers, demodulators, amplifiers and discretes in a highly dense form factor with ultra-low interconnect parasitics.

Advanced SiPs integrate disparate technologies, such as a small microprocessor with embedded memory, a sensing element such as a MEMS device or image

MEMS and Sensor Application	Accelerometer, Gyroscope, Magnetometer, IMUs	Visible Light, Proximity, Ambient Light, Depth Sensing, IR	Microphones, Pressure, Gas, Temperature, Humidity, Environmental, Gesture	Sensor Fusion and IoT
Package Type	**Overmolded**	**Exposed Die Surface**	**Cavity Package**	**Hybrid Cavity Package**
SOIC				
MLF®/QFN				
ChipArray® LGA/FPBGA				

Figure 3. MEMS and sensor standard package platforms.

sensor, RF die and power management ICs in a very small form factor. In these designs, it is not unusual to find various different interconnects such as wire bond, flip-chip and WLCSP BGA along with surface mounted components.

The laminate-based advanced SiP qualifies as one of the Big Five packaging technologies because it fits the bill for new market growth areas, providing a great deal of value in terms of form factor and increased functionality at a cost point that accelerates product penetration in new and existing markets. For example, laminate-based SiP solutions can enable miniaturized cost effective solutions in the consumer and industrial IoT space, since they integrate increased functionality and component counts in very small form factors.

Laminate-based SiP solutions that are currently in production achieve the lowest form factor at cost and performance points that address market needs in RF, storage, automotive, IoT and power segments. In addition, a core design kit enables customers to do module and substrate design and also supports system modeling, characterization and full turnkey services to achieve the smallest form factors and fastest time to market.

Wafer-based Advanced SiP

Similar to a laminate-based advanced SiP, a wafer-based advanced SiP allows for the integration of complex and disparate technologies, but meets the higher performance requirements for bandwidth, form factor and density requirements in high-performance computing (HPC), IoT, mobility and automotive segments. In addition to integrating basic microprocessors, sensing elements (MEMS or image sensors), RF dice and power management ICs, a wafer-based advanced SIP can integrate memory (high bandwidth memory (HBM), Hybrid Memory Cube (HMC), and others), ASIC devices and high-performance processors, such as GPUs and FPGAs. This final segment of the Big Five is the technology that serves the widest scope of applications.

The wafer-based advanced SiP is currently targeted for high-end devices and is still in the early introduction phases to the industry. It effectively addresses system-scaling needs and can help offset or delay the need for next-generation Si node based products. Its initial market entry points are HPC, memory and high-end mobility. Over time, however, more devices will take advantage of wafer-based SiP technology to enable extreme form factor reductions and increased product performance at lower power.

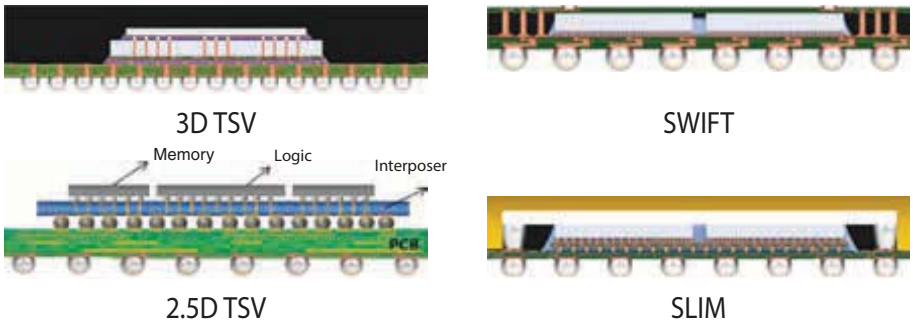


Figure 4. Wafer-based SiP offerings.

While laminate-based SiP leverages the existing die scale infrastructure, wafer-based processes differ significantly from laminate-based processes and require investment in wafer processing tooling. Wafer-based SiP replaces and/or complements the laminate substrate, providing RDL line/space (l/s) features down to 1 μm x 1 μm. A wafer-based SiP RDL can scale to fab back end of line (BEoL)-like dimensions, whereas traditional laminate-based advanced SiPs are currently limited to 10 μm x 10 μm l/s. Therefore, wafer-based SiP systems provide the best-in-class (BiC) scaling capability and have the ability to scale to fab-like dimensions.

There are increased costs associated with wafer-based SiP due to the complexity of the products produced. One of the contributors to the increased costs compared to laminate-based advanced SiP is the capital expenditures (CapEx) required to build a platform for wafer-based processes in Class 1 or Class 10 cleanrooms. Fab-like infrastructure and additional toolsets including those used for traditional front-end processes such as physical and chemical vapor deposition (CVD) tools, chemical mechanical planarization (CMP) tools and temporary bond/debond systems, contribute to the increased upfront costs required to enable wafer-based SiP platforms. As the tools and factories depreciate, the manufacturing costs of wafer-based advanced SiPs will be reduced, enabling a wider set of applications to take advantage of the form factor reduction and significant product performance increases.

Package configurations in the wafer-based advanced SiP family include high-density fan-out wafer-level packages such as the SWIFT™ and SLIM™ product lines. These configurations use a "die last" approach that minimizes the yield loss risk prevalent in the complex die first WLFO packages. SWIFT is expected to ramp to production in the next few quarters and become a predominant driver of wafer-based advanced SiP products. The SLIM and SWIFT small body sizes have passed chip-package interaction (CPI) qualifications, with large body sizes in development. Also on the wafer-based advanced SiP roadmap are 2.5D interposer and 3D IC stacks. The 2.5D TSV is available today, having been qualified since 2013. Working with ecosystem partners provides a seamless supply chain and qualified Si portfolio and also enables co-design by providing design kits for each of the wafer-based SiP platforms. Figure 4 shows these packaging approaches.

Advanced Packages for Today and the Future

The mobility market is driving form factor reduction and high-density interconnects for multi-die integration. In the HPC, networking, deep learning and GPU applications, wafer-based advanced SiPs address the power, memory bandwidth and latency issues of new devices coming to the market in the next couple of years. The 2.5D, 3D, SLIM and SWIFT technologies can potentially help OEMs and fabless companies delay migration to the next node by enabling system-scaling approaches through wafer-based SiP technology.

Wafer-based advanced SiPs round out the Big Five portfolio, allowing continued innovative choices that will help achieve the best performance, form factor and value-to-cost ratio for any application. ◆