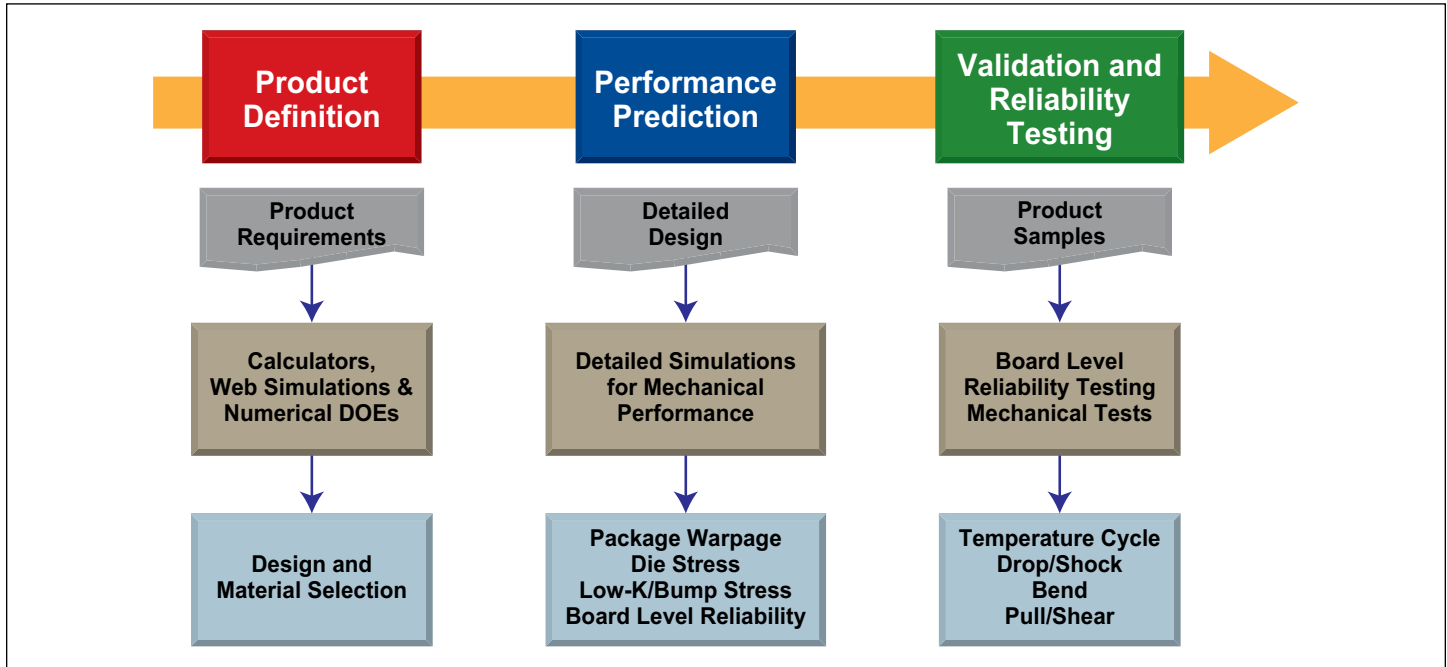


Mechanical Characterization

Mechanical Package Characterization

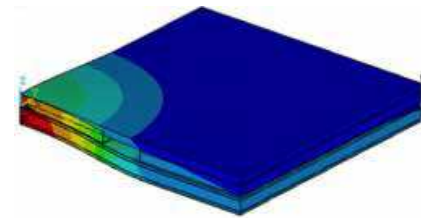
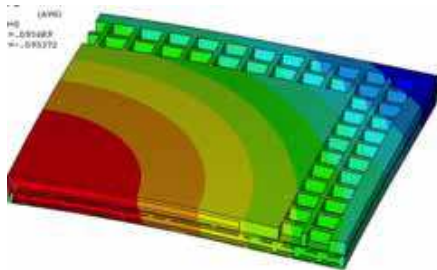
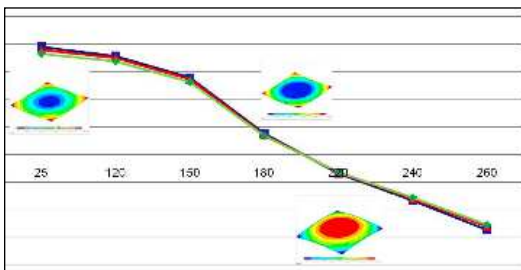
Mechanical characterization is an integral part of Amkor's product development and characterization. During product definition stage, quick calculators and numerical DOEs are used to select design attributes and materials meeting performance and reliability requirements. A more detailed set of simulations are then performed on actual designs incorporating substrate and die details. Finally, simulation results are validated with actual warpage measurements and reliability testing on engineering samples.



Mechanical Simulation Capabilities

Package Warpage

- One of the key considerations for IC packages, especially thin 3D and PoP packages
- Warpage is caused by the CTE mismatch of various materials involved and is typically temperature dependent
- Excessive warpage can cause shorts, non-wets or de-wets during the board assembly process
- Amkor offers package warpage prediction using a finite element method for all package types. Warpage predictions are provided for both room and elevated temperatures to help optimize package design and material parameters.



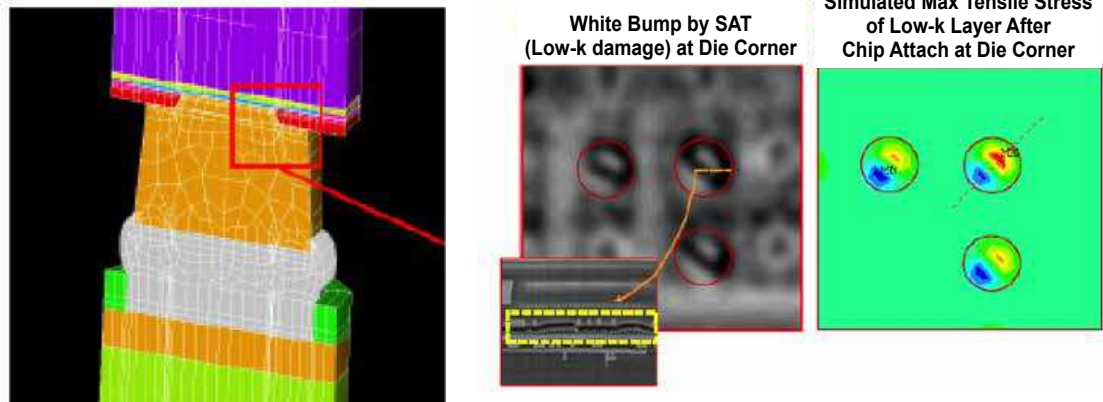
Visit Amkor Technology online for locations and to view the most current product information.



SS23B
Rev Date: 1/13

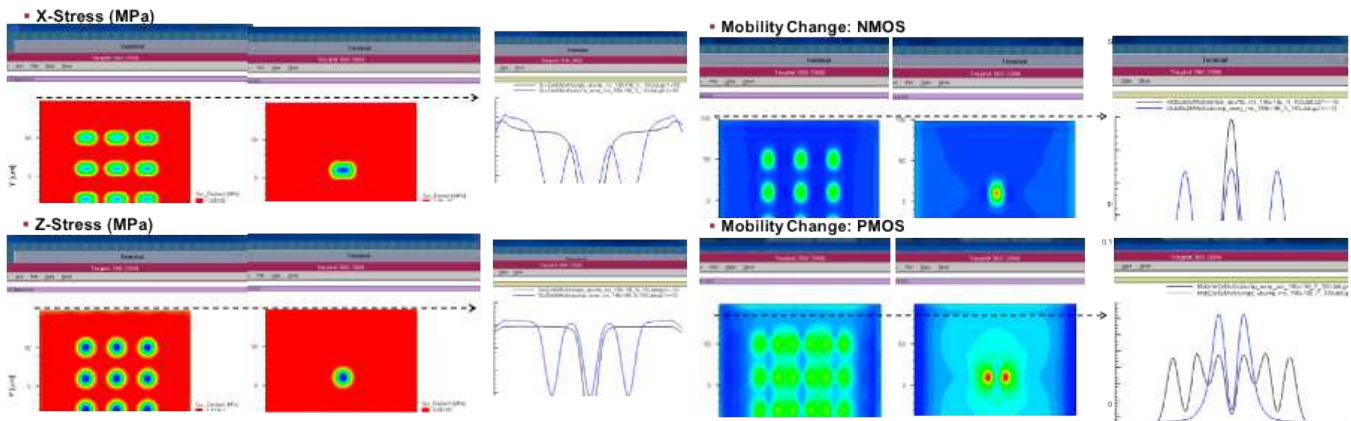
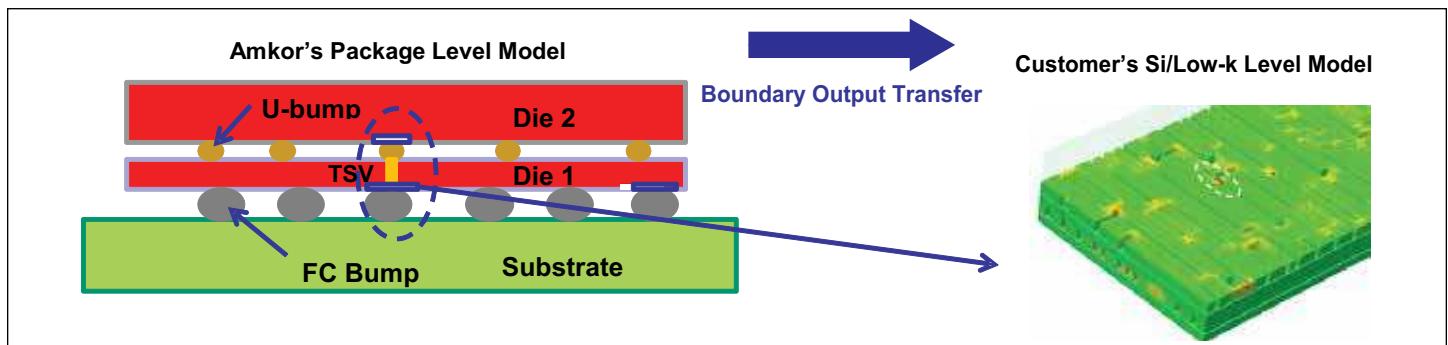
Interconnects and Die/Low-k Stress

- Prediction of stress due to reliability testing or from assembly processes
- Stress prediction at different interfaces or bulk materials such as die, ELK, UBM, Cu pillar, solder bump, substrate Cu trace
- Correlation of stress levels to various failure modes and locations to avoid potential reliability concerns



Chip Package Interaction

- Advanced chip/Low-k design performance can be affected by the external stress/strain load generated from the package
- Amkor is capable of setting up the package level mechanical model and provides the specified boundary loading results to customers for their in-house Si/Low-k level model/design tool. This helps in optimizing design up-front and facilitates chip-package co-design.



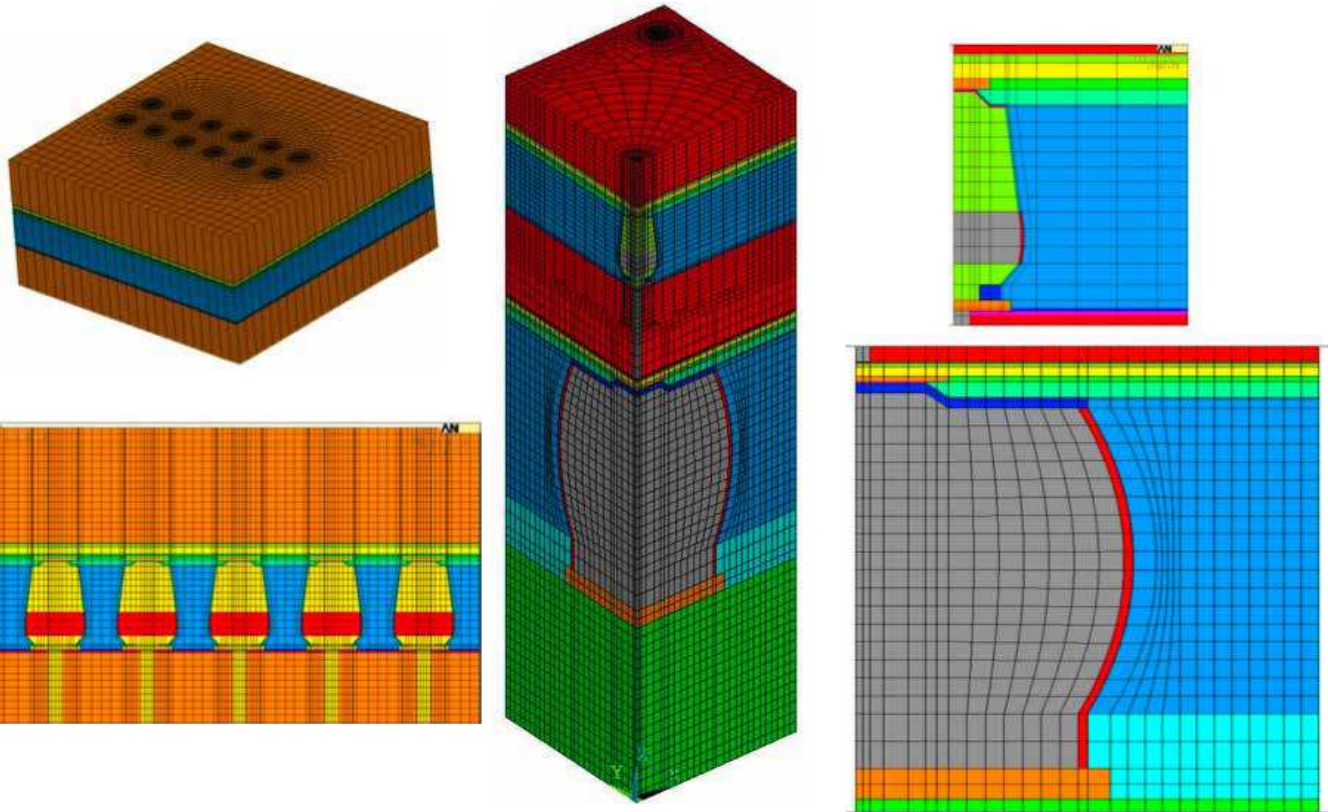
Visit Amkor Technology online for locations and to view the most current product information.



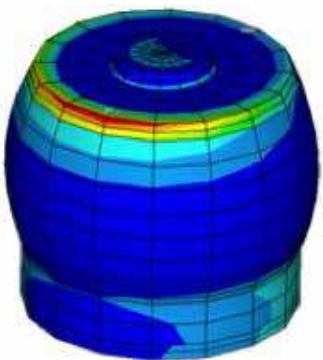
SS23B
Rev Date: 1/13

3D Package Model

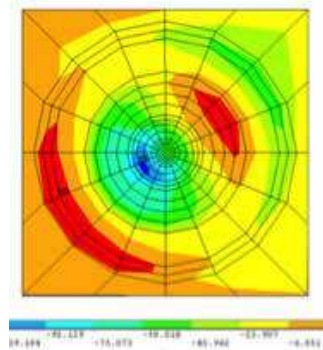
- For Thru-Silicon-Via (TSV), Package-on-Package (PoP), Thru-Mold-Via (TMV[®]), Wafer-Level-Package (WLP) and System-In-Package (SIP)
- Simulations for design and material impact on stress at TSV, μ -bump, FC bump, RDL layer for potential failure as well as warpage prediction for 3D IC and 3D package configurations



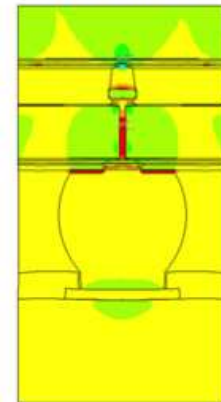
Bump Stress



Low-k Stress

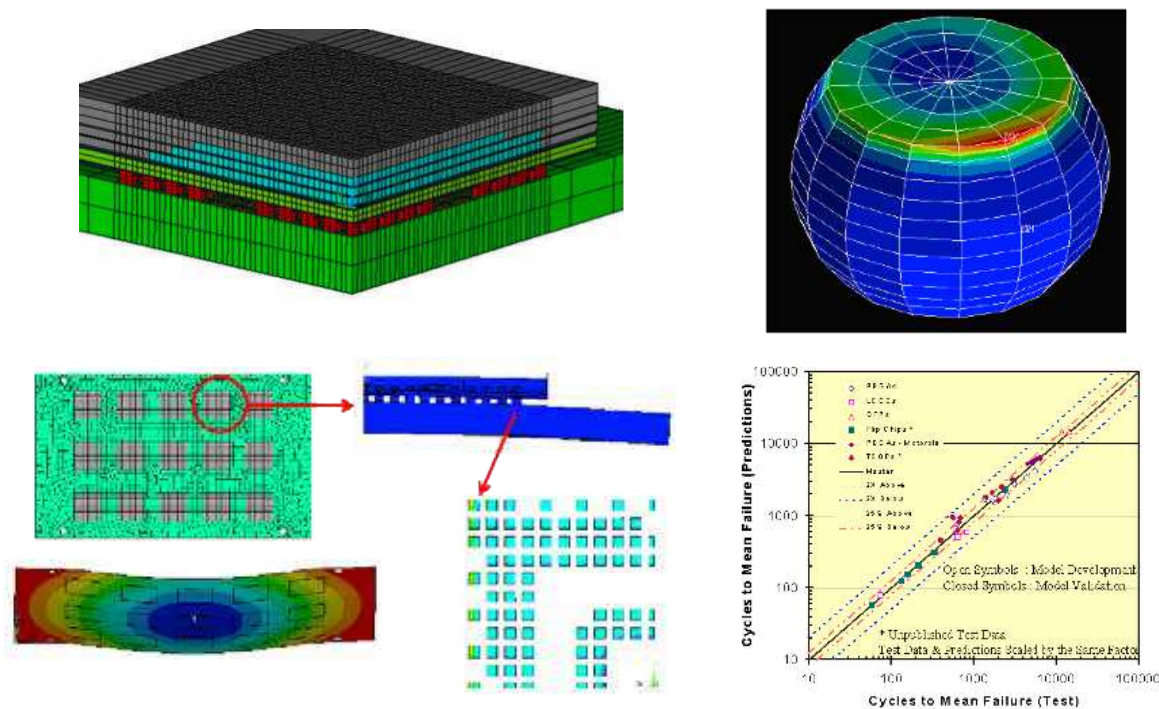


TSV Stress



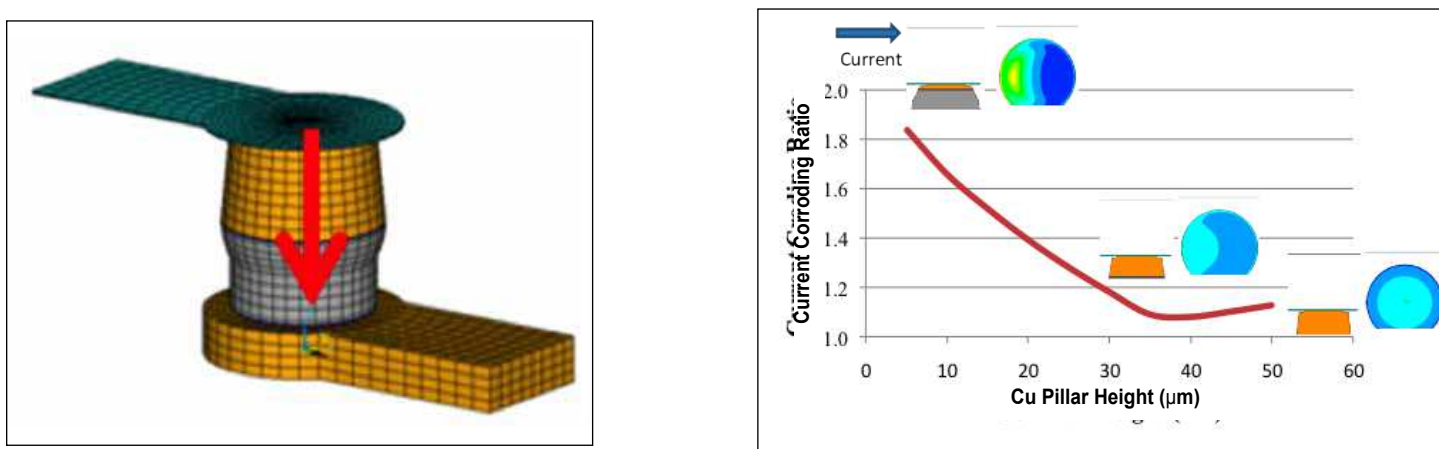
Board Level Reliability (BLR) Prediction

- Solder joint life prediction for temperature and power cycling: finite element based simulation provides a quick estimation of expected reliability and is used extensively in the pre-design stage. The life prediction approach correctly predicts the location of critical solder joints and location of failure (board or package side) with a high degree of accuracy for actual values.
- Board level drop test simulation: provides relative comparison for package material and design attributes



Electro-migration Model

- Provides estimation of current density distribution within an interconnect
- Simulations are used to determine the impact of bump design on current density distribution and potential electro-migration reliability



Visit Amkor Technology online for locations and to view the most current product information.

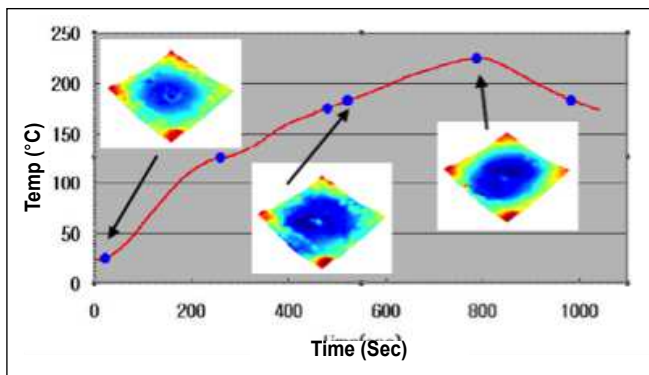


SS23B
Rev Date: 1/13

Mechanical Test and Measurement Capabilities

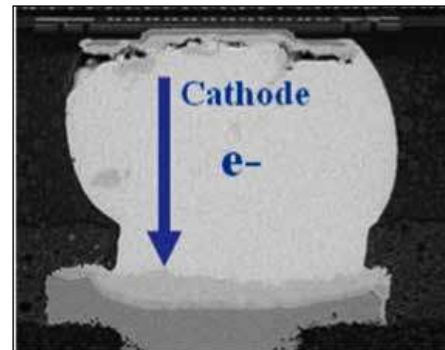
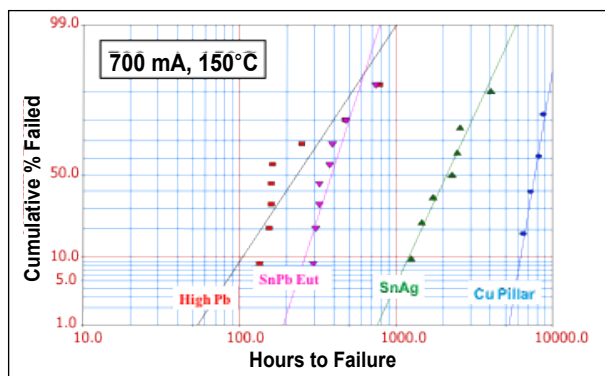
Warpage Shadow Moire Measurement

- Full compliance with JEDEC JESD22B112 standard
- Warpage at room and elevated temperatures



Electro-migration Test

- Test capability to test low and high current applications
- Data collected on Flip Chip bumps, μ -bumps, Cu Pillars and WLCSP



Board Level Reliability

Board level reliability is one of most important aspects of package selection. Electronic assemblies experience varied field use stress conditions during their useful life and package-to-board interconnects are required to survive these conditions. As part of our strategy to provide complete packaging solutions to our customers, Amkor offers solder joint reliability characterization of all package styles.

Visit Amkor Technology online for locations and to view the most current product information.



SS23B
Rev Date: 1/13

Temperature Cycle Tests

Amkor employs the following three temperature cycle test conditions for board level reliability, depending on the intended end use application of the package. All three of these conditions comply with IPC-9701 specifications. In-situ electrical testing is performed to identify failures.

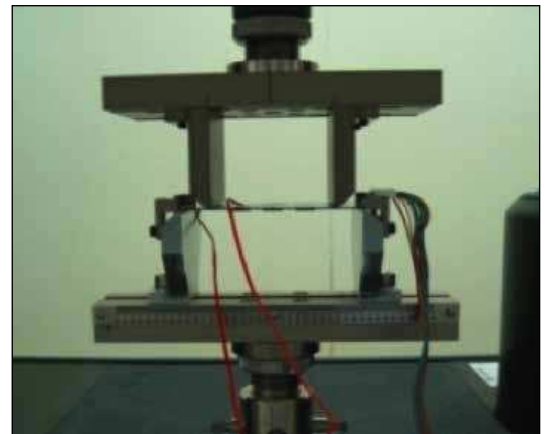
Condition (°C)	Min. Temp. (°C)	Max. Temp (Minutes)	Ramp Up Time (Minutes)	Ramp Down Time (Minutes)	High Temp. Dwell (Minutes)	Low Temp. Dwell (Minutes)	Cycle Duration (Minutes)
TC1	-40	125	15 (+5/-0)	15 (+5/-0)	15 (+0/-5)	15 (+0/-5)	60
TC2	-55	125	2 - 3	2 - 3	12 - 13	12 - 13	30
TC3	0	100	10(+2/-0)	10 (+2/-0)	10 (+0/-2)	10 (+0/-2)	40

Board Level Drop Tests

This test is implemented to provide a controlled environment to reproduce the interconnect failure mode commonly experienced during drop of handheld electronic systems (e.g., mobile phones, PDAs, etc.). The testing is conducted as per JEDEC standard (JESD22-B111). Amkor is also certified by Nokia and Motorola for testing according to their test methods.

Cyclic Bend Test

The cyclic bend test consists of bending the printed circuit board assemblies using a 4-point bend test fixture. This test may be used to reproduce solder joint failures experienced in package mounted on key pads.



Visit [Amkor Technology](http://www.amkor.com) online for locations and to view the most current product information.



With respect to the information in this document, Amkor makes no guarantee or warranty of its accuracy or that the use of such information will not infringe upon the intellectual rights of third parties. Amkor shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it and no patent or other license is implied hereby. This document does not in any way extend or modify Amkor's warranty on any product beyond that set forth in its standard terms and conditions of sale. Amkor reserves the right to make changes in its product and specifications at any time and without notice. © 2013, Amkor Technology Incorporated. All Rights Reserved.

SS23B
Rev Date: 1/13