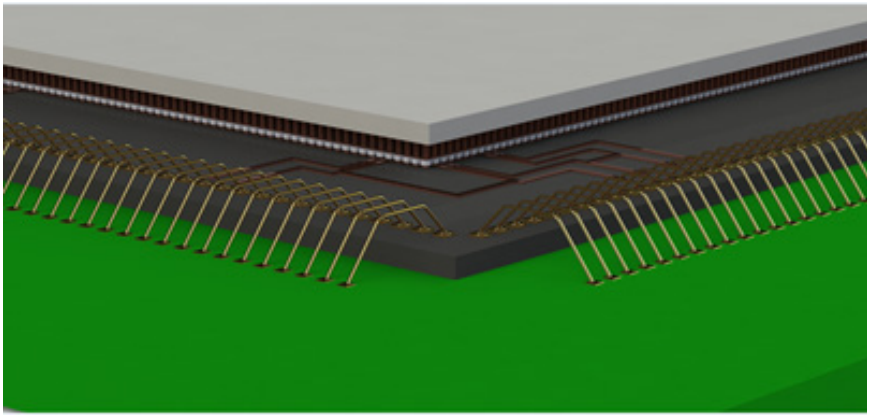
Chip-on-Chip (CoC)

POSSUM™ Technology

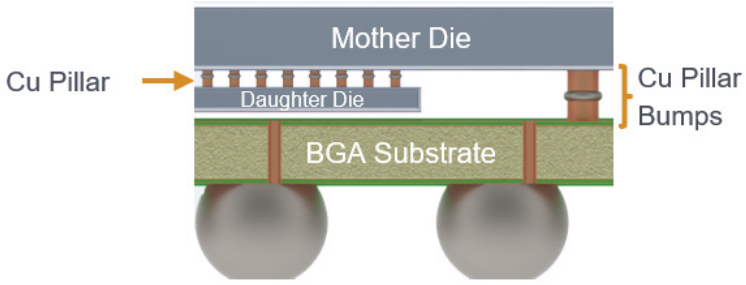
Chip-on-Chip is a packaging technology designed to electrically connect two (or more) dice together, without the need for TSV (Through Silicon Vias). Electrical interconnection is achieved via fine flip chip interconnects, sub 100 µm, in a face-to-face configuration.

The mother die can then be connected to the package using flip chip bumps or wire bonds, typically at a coarser pitch to match the package. The two (or more) dice can now communicate more efficiently at faster speeds, with larger frequency bandwidth, reduced electrical resistance (R), inductance (L) and capacitive resistances, and at a lower cost than TSV. In the wire bond package interconnect scheme, the CoC is connected to the package substrate via perimeter wire bonds on the mother die.



Conceptual Illustration of CoC Attached to Package Substrate Using Wire Bonds

The CoC may also be connected to the package via POSSUM™ configuration. In this configuration, the mother die uses fine flip chip interconnects, sub 100 µm, and coarser pitch bumps to interconnect to the package substrate. The daughter dice is thinned to allow for underfill clearance during package assembly. An added benefit of the POSSUM™ configuration is the reduced Z-height of the CoC and overall package.



Conceptual Illustration of POSSUM™ Assembly

CoC Value Proposition

POSSUM™ technology provides packaging advantages.

- Package size and form factor reduction
- 2.5D/3D integration
- Increased functionality
- Performance improvements
  - Lower power dissipation
  - Higher density
  - Faster systems

Primary Focus

- Leverage fine pitch CuP bumping and die stacking capabilities in production
- Provide alternate method for heterogeneous integration

Applications

- MEMS, automotive, mobile, networking, power management, optoelectronics, artifical intelligence
- Formats: CSP, PBGA, WLCSP, FCBGA, FusionQuad®

Amkor Technology®

Chip-on-Chip (CoC)

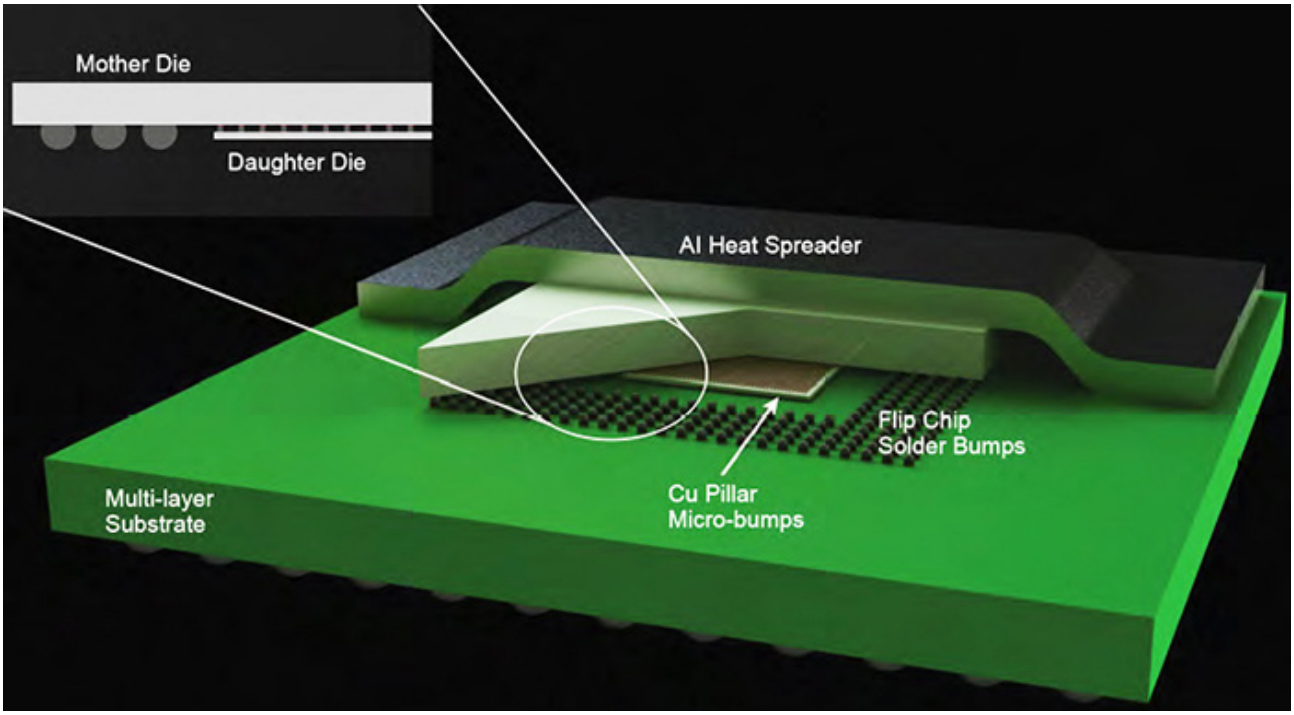
Amkor has taken a proactive and strategic approach in the research and development of CoC. The technology has proven to be beneficial and advantageous from both a cost and technical standpoint. The CoC packaging method has evolved from the existing technologies of flip chip and Fine Pitch Copper Pillar (FPCP). Amkor has extensive experience in CoC mass production and the technology uses existing infrastructure that is readily available, with minimum supplemental capital investment.

300 mm Chip on Wafer (CoW)

Chip on Wafer (CoW)

Complementary to CoC, Chip on Wafer (CoW) has been developed and is in production at Amkor. In the CoW approach, the mother wafer is not sawn, but instead is used as the substrate, populated with sawn daughter dice. In addition to the advantages of CoC, CoW provides the added benefit of chip set test and simplified logistics. Both 200 and 300 mm wafers are supported with a wide range of die sizes and chip stack thicknesses.

This technology has been developed over the course of several years, in parallel with engaging key alpha customers for strategic market segments. This has allowed Amkor to support a wide range of products in a variety of application areas in the micro sensors, automotive microcontroller, wireless, optoelectronics and mobile arena.



Cross section of High End FCBGA Lidded Package Using CoC POSSUM™ Interconnect

Visit amkor.com or email sales@amkor.com for more information.