



Small Outline IC Package (SOIC)

SOIC is a leadframe based, plastic encapsulated package that is well suited for applications requiring optimum performance in IC packaging. This industry standard package runs in very high volume and provides value added, low cost solutions for a wide range of applications.

Features

- Cu wire interconnect for low cost
- Standard JEDEC package outlines
- Multi-die production capability
- Turnkey test services, including strip test options
- Green materials are standard – Pb-free and RoHS compliant
- Stealth dicing (narrow saw streets)
- Larger/higher density leadframe strips
- Leadframe roughening for improved MSL capability

Services and Support

Amkor has a broad base of resources available to help customers bring quality new products to market quickly and at the lowest possible cost.

- Full package characterization
- Thermal, mechanical stress and electrical performance modeling
- Turnkey assembly, test and drop ship
- World class reliability testing and failure analysis

Visit [Amkor Technology](http://www.amkor.com) online for locations and to view the most current product information.

SOIC

Thermal Performance

Forced Convection, Single-layer PCB

Pkg	Body Size (mm)	Pad Size (mm)	ΘJA (°C/W) by Velocity (LFPM)		
			0	200	500
8 ld	4.9 x 3.8	2.3 x 2.3	153.3	128.5	115.5
20 ld	12.8 x 7.6	5.1 x 4.1	83.2	65.7	57.5

JEDEC Standard Test Boards

Forced Convection, Multi-layer PCB

Pkg	Body Size (mm)	Pad Size (mm)	ΘJA (°C/W) by Velocity (LFPM)		
			0	200	500
8 ld	4.9 x 3.8	2.3 x 2.3	112.7	103.3	97.1

Pre-JEDEC Standard Test Boards

Electrical Performance

Pkg	Body Size (mm)	Pad Size (mm)	Lead	Inductance (nH)	Capacitance (pF)	Resistance (mΩ)
8 ld	4.9 x 3.8	3.6 x 2.3	Longest	1.25	0.263	8.2
–	–	–	Shortest	0.718	0.218	5.1

Simulated Results @ 100 MHz

Reliability Qualification

Amkor package qualification uses three independent production lots and a minimum of 77 units per test group. All testing includes JSTD-020 moisture preconditioning.

- Moisture Sensitivity Characterization: JEDEC Level 1, 85°C/85% RH, 168 hrs; JEDEC Level 3, 30°C/60% RH, 192 hrs
- uHAST: 130°C/85% RH, No Bias, 96 hrs
- Temp Cycle: -65°C/+150°C, 500 cycles
- High Temp Storage: 150°C, 1000 hours

Process Highlights

- Au plated PCC wire is standard, Au and Ag wire available
- Wafer backgrinding services available
- Multiple die and die stacking capability
- NiPdAu (PPF) lead finish is standard, Matte Sn is optional
- Laser mark on package body



SOIC

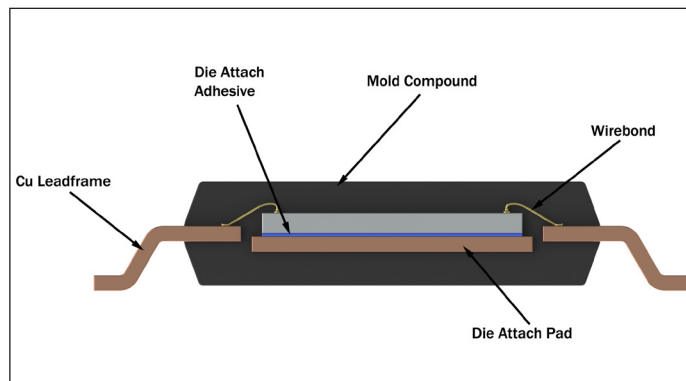
Test Services

- Program generation/conversion
- Wafer probe
- Burn-in capabilities
- -55°C to +165°C test available
- Strip test available

Shipping

- Clear anti-static tube, 20 inch
- Tape and reel
- Dry pack
- Drop ship

Cross-section SOIC



Configuration Options

SOIC Nominal Package Dimensions (inches)

Package Type	Lead Count	Body Width	Body Length	Body Thickness	Standoff	Overall Height	Lead Pitch	Tip-to-Tip	JEDEC
SOIC Narrow	8	0.150	0.194	0.058	0.006	0.064	0.050	0.236	MS-012
	14	0.150	0.342	0.058	0.006	0.064	0.050	0.236	MS-012
	16	0.150	0.391	0.058	0.006	0.064	0.050	0.236	MS-012
SOIC Wide	8	0.208	0.208	0.071	0.004	0.075	0.050	0.311	N/A
	16	0.300	0.407	0.092	0.009	0.101	0.050	0.406	MS-013
	18	0.300	0.456	0.092	0.009	0.101	0.050	0.406	MS-013
	20	0.300	0.505	0.092	0.009	0.101	0.050	0.406	MS-013

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