

Wafer Bumping

Wafer Bumping Processes and Die Level Interconnect Technology Services

The electrical and mechanical connection between a die and substrate is one of the most critical elements of any flip chip package or Wafer Level Package (WLP) structure.

Predominantly lead-free solders are used to create these bump connections and must exhibit superior adhesion to the die, minimal resistance, and result in high assembly yields. These solder bumps are formed by using either thin film metal deposition, plating or ball loading techniques.

Amkor offers state-of-the-art capabilities in electroplated bumping and various types of Wafer Level Chip Scale Packaging (WLCSP) in multiple strategic locations. Our China, Korea, Portugal and Taiwan bumping operations are co-located with wafer probe, assembly and final test, enabling Amkor to provide complete “turnkey” flip chip and WLCSP solutions in these key geographic locations. In addition, these facilities are situated adjacent to major foundry sources, and provide customers reduced time-to-market with integrated factory logistics.

These Amkor facilities have world-class bumping lines with HVM production capability. 200 mm and 300 mm lead-free and Cu pillar solder compositions (all low alpha) are production certified. Service offerings include repassivation and single and multi-layer redistribution processes for both flip chip and WLCSP applications.

These facilities offer economy of scale as both plated bump (solder/CuP bump) and WLCSP/Wafer Level Fan-Out (WLFO) continue to grow. This combination of technology and manufacturing capabilities is unparalleled in the subcontract manufacturing industry.

TECHNOLOGY DEVELOPMENT

Amkor maintains strong initiatives in the area of technology development to further support customers' future needs. Continuous improvement programs are in place to optimize and cost-reduce wafer bumping processes.

Amkor's technology leadership continues to advance flip chip technology as part of our broad portfolio of over 1000 packages. We continue to partner with leading companies to bring new flip chip products to market quickly. We have the vision and breadth to move flip chip interconnect off the drawing board and into production across a wide range of package formats.

- ▶ Electroplating capabilities will support fine pitch bumping and copper pillar structures
- ▶ Higher performance repassivation materials and low-temp cure repassivation
- ▶ Thin profile WLCSP and multi-redistribution layer product
- ▶ Providing diversity in WLFO
- ▶ WLCSP die size support to greater than 144 I/Os and 0.3 mm pitch
- ▶ Automotive qualified



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Bumping Process Specifics

Amkor's bumping process is production certified in the full package size range, from WLCSP up through large die Flip Chip BGA (FCBGA).

All factories are ISO/TS16949 certified.

Wafer Size	200 mm, 300 mm
Solder Compositions	98.2 Sn/1.8 Ag (All Available As Low Alpha: <0.002 cts/hr/cm ²), SnAgCu, Doped Alloys
Pad Pitch Lower Limit	50~500+ μ m
Repassivation Coatings	Polyimide, PBO, Low Cure Polymers
Redistribution Materials	Plated Copper



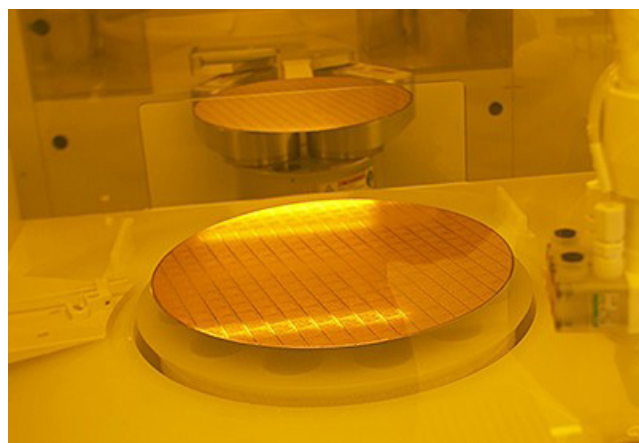
Related Processes/Services

Wafer bumping and WLCSP use many of the same basic process steps in production. Key WLCSP developments have resulted in improved wafer level technology known as CSP^{nl}.

CSP^{nl} combines plated copper technology and advanced photopolymers to produce the industry's most robust wafer level solutions. CSP^{nl} is available down to 0.3 mm pitch and supports a range of solder volumes to meet customer requirements.

Closely related to both bumping and WLP production is "die processing" capability, which consists of process steps that transform either bumped or WLCSP product from wafer form into die form.

Die processing typically involves backgrind, backside coat, test, singulation, inspection, tape and reel, and pick-and-place. Amkor offers these full turnkey services to support our customers in China (C3), Korea (K5), Portugal (E1) and Taiwan (T3/T6) factories.



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