Developing a Theta$_{JC}$ Standard for Electronic Packages

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Abstract

Theta jc data are commonly reported for most electronic packages. However, a JEDEC standard that specifies best practices for performing steady-state Theta jc measurements is not yet available. Presented in this study are recommendations for making consistent Theta jc measurements, including criteria for mounting the case thermocouple, predicting the impact of TIM II material, bond line thickness, effect of heat-sink construction materials and testing variability introduced by different test engineers. At a critical Theta jc value, predictions show that case temperature measurements must be made using a thermocouple embedded into the case of the package.

Keywords

Theta jc, ΘJC, JEDEC, Electronic Package, Measurement, Experimental, Thermal

Nomenclature

A	Area (mm^2)
A_{eff}	Effective area (mm^2)
A_{SPRD}	Spreading area (mm^2)
L	Bond line thickness (mm)
K	Thermal conductivity (W/mm/k)
P_{el}	Electrical power (W)
Q	Heat flowing through lid (W)
S	Gap between active surface of die and case (mm)
T_c	Case temperature (°C)
T_j	Junction temperature (°C)
δ	Gap between die backside surface - package case (mm)
Θ_{JC}	Theta JC, junction-to-case resistance (°C/W)
Θ_{JS}	Theta JS, junction-to-sink resistance (°C/W)

1. Introduction

Testing standards are used to provide a common reference for comparing experimental data. The goal of any standard is to enable test labs to follow the same procedure and measure approximately the same data within an agreeable level of uncertainty. Since testing methodologies have an influence on measurements, it is important that a standardized method be developed that is accepted by the thermal community. The standard should not create a financial burden on test labs by requiring the purchase of expensive instrumentation or require complex methods to evaluate Θ_{JC}. The charter for the JEDEC Thermal Standards Committee, JC-15, is to facilitate discussion of details related to the development of standards, offer a forum for peer review and to provide a depository for standards. The guiding principles for developing a standard include: it should be useful, understandable by the general technical community, scientifically sound and provide a method that is reproducible.

The purpose of this paper is to document some of the considerations used to develop a steady-state testing method for measuring the junction-to-case thermal resistant, Θ_{JC}, in electronic packages. Attention is given to quantify the reproducibility of measurements made at different laboratories. In addition, instrumentation and testing hardware were selected based on the availability at most testing laboratories.

Θ_{JC} is defined in equation (1) as the difference between the junction temperature (measured on the active side of the die) and the case temperature (measured on the exposed side of the package in the path of the primary heat flow direction) divided by the heat flowing through the case of the package.

$$\Theta JC = \frac{T_j - T_c}{Q} \quad (1)$$

This definition follows the common expression used to evaluate thermal resistance measured between two nodes, i.e., the junction and the case. Packages that have low Θ_{JC} provide lower resistance to the transfer of heat between the junction on the die to the case of the package and therefore experience a smaller temperature rise. Examples of low Θ_{JC} packages are the flip chip ball grid array (FCBGA) package and packages where die are mounted to a copper slug, e.g. power small outline package (PSOP). Higher Θ_{JC} packages typically have small die (e.g. less than 5mm x 5mm) and are encapsulated with lower thermal conductivity mold compounds. Examples of higher Θ_{JC} packages include the carrier array ball grid array package (CABGA) or flip chip scale package (fcCSP).

JEDEC test standard JC51-1[1] specifies the methodology for measuring the junction temperature on a thermal test die. Functional die add complexity for measuring Θ_{JC} because they typically do not deliver a uniform power map as required by JC51-1 and seldom have a temperature sensor located at the hot spot on the die. To reduce complexities in developing a steady-state Θ_{JC} standard, it is recommended that it only be applied for packages that are powered with a thermal test die.

Measuring the case temperature generates the most discussion during JEDEC standard meetings. JEDEC committee members have differing opinions on the best method for measuring the case temperature. Some of the techniques include embedding a thermocouple into the cold plate, touching the case with a temperature probe through a hole normal to the cold plate surface, optically measuring the

case temperature through a hole in the cold plate or embedding a thermocouple into the case of the package. For an overview of these methods, see [2]. A recommendation for measuring the case temperature is provided in this study.

The electrical power, P_{el}, supplied to the package is measured using four-point connections to the heater [1]. However, less than 100% of the electrical power supplied to the die passes through the case. An experimental method was developed to account for the heat loss using a calorimetry bar attached to the cold plate to determine Q experimentally [3]. Although this method was useful as an explicit method for measuring Q, it has practical limitations due to testing difficulties such as reaching a steady-state conditions in a reasonable amount of time (less than approximately 30 min). The best approach for reducing heat is to insulate the back of the mother board with a backing plate inserted between the test board and the loading weight (see Figure 2) and by restricting air flow around the test board. An estimate should be provided on the heat-loss and difference between Q and P_{el}.

Opponents of steady-state Θ_{JC} method suggest avoiding it all together by using a transient method [4] to overcome the necessity for measuring the case temperature. The transient method, as specified by JESD 51-14 [5], is a useful method for measuring Θ_{JC} when the heat flow path is primarily in a single direction, i.e. from the die directly into the case. Examples of this style of package include the TO-220 or a quad-flat pack no-leads (QFN). For larger packages, such as the FCBGA or CABGA, the transient heat flow path is three-dimensional including heat flow into the substrate copper planes and through the solder balls. For packages having multiple heat flow directions, the transient Θ_{JC} standard is not valid. For many package styles, a steady-state method is needed to overcome the uncertainties introduced by multi-direction heat flow.

2. Experimental Testing

A systematic measurement methodology is required to measure Θ_{JC} accurately including; developing heat-sink designs, data acquisition system, instrumenting the package and heat-sinks, calibrating temperature devices, performing the measurements and reporting the results. In theory, if two labs follow the same testing methodology, they should measure approximately the same Θ_{JC} value. Each block listed in Figure 1 has an impact on the measured Θ_{JC} value.

Figure 1. Θ_{JC} testing procedure.

A series of round-robin tests were planned to understand the reproducibility of Θ_{JC} test data collected by different test engineers. To facilitate simplicity in testing, the chosen heat-sink was constructed using commonly available materials, see Figure 2. A CPU cooler with a sink-to-ambient resistance of 0.12°C/W was selected rather than a cold plate to avoid procuring a liquid cooled chiller. The JEDEC board was aligned and centered over the CPU cooler using two dowel pins to ensure a repeatable mounting position for the JEDEC board. An insulation block made from 19mm thick phenolic plate was placed over the backside of the test board to reduce heat-loss from the mother board.

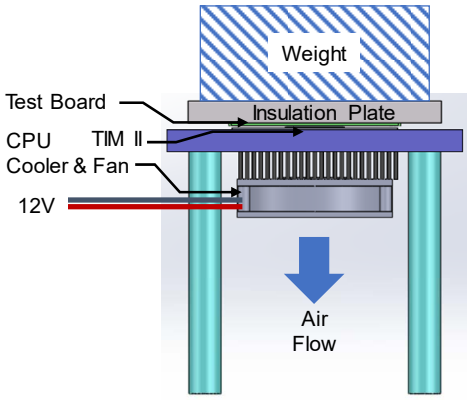

Figure 2. Experimental test system.

Three different packages were selected for this study, see Table 1. The first package tested was a carrier array ball grid array (CABGA) package. It has a higher thermal resistance due to the low thermal conductivity enhanced mold compound (EMC) used to encapsulate the package. The second package tested is a thermally enhanced plastic ball grid array package with a drop-in heat spreader (TEPBGA2). A lower Θ_{JC} was achieved due to its larger die, heat spreader and thinner EMC gap. Two different thermal conductivity EMCs were tested on the TEPBGA, 0.9W/m/K and 2.5W/m/K. The third package tested is a flip chip ball grid array package (FCBGA). This package has the lowest Θ_{JC} due to its larger die size and high conductivity and thin layer of thermal interface material (TIM) between the lid and the die. All packages were soldered to a JEDEC multi-layer test board. The package and mother board combination is referred to as the thermal test vehicle (TTV).

Table 1. Package during the round-robin test.

	CABGA (A)	TEPBGA2 (B)	FCBGA (C)
Pkg	δ ~ 0.40mm K = 0.9W/m/k	δ ~ 0.20mm K = 0.9, 2.5 W/m/k	δ ~ 0.035mm K = 3.5W/m/k
Θjc	7°C/W	1.7, 2.5°C/W	0.07°C/W
Body	12mm x 12mm	40mm x 40mm	40mm x 40mm
Die	7.8mm x 7.8mm	10.2mm x 10.2mm	16mm x 16mm
Pres.	68KPa	56KPa	51Kpa
#	(6)	(6)	(6)

Two methods were used to sense the case temperature. The first method embedded a 40 gauge thermocouple into the lid of the package as shown in Figure 3. A 250µm x 300µm groove was milled into the case of the package. Next, a type K thermocouple was inserted into the groove and covered with high thermal conductivity silver epoxy (k~7.5W/m/k). Finally, once the epoxy was cured, the top surface of the package was planarized so that the epoxy fill was smooth with the top surface of the package.

The second method for sensing the case temperature was to cut the same groove into the surface of the heat-sink and follow the aforementioned thermocouple assembly procedure.

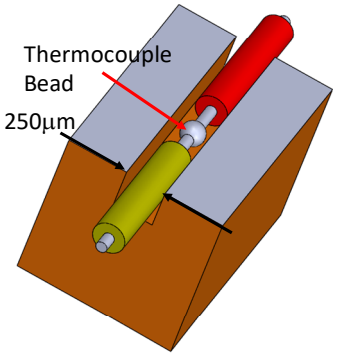

Figure 3. Embedded Type K thermocouple (40 gauge) installed in the case or heat-sink.

The embedded heat-sink thermocouple was used to sense the case temperature for the CABGA packages and the low conductivity EMC TEPBGA2 packages. The embedded thermocouple in the lid was used to sense the case temperature for the high conductivity EMC TEPBGA2 packages and FCBGA packages. Six packages were tested for each package type. Weights were applied to the back insulation plate to provide a clamping pressure (based on package contact area) to the heat-sink. The applied contact pressures are listed in Table 1.

The same testing procedure was followed by all test engineers. Electrical connections were made to the mother board and thermocouples were connected to the data acquistion system. The required weights were placed on the backside of the mother board. The CPU cooler fan was powered using a fixed 12V source.

A high thermal conductivity silver filled grease (K~9W/m/K) was selected for the TIM II. An initial bond-line thickness (BLT) was approximately 70µm and was created by spreading the TIM II on the heat-sink with a razor blade supported by two strips of kapton tape each having a thickness of approximately 70µm. The actual BLT will be thinner as the grease presses out and away from the package mating surface under the force of the weights placed on the back-side of the mother board. The final BLT may be determined by the warpage of the packages and the filler size of the TIM II. The minimum TIM II BLT thickness was estimated to be approximately 30µm by trapping a thermal grease sample between the fingers of a caliper and measuring its thickness.

Steady-state was achieved when the junction and case temperatures reached a stable condition such that the variation was less than ±0.1°C measured over a 5 minute period and the change in temperature with time did not show an increasing or decreasing trend. Before running the next test, the packages were removed from the heat-sink and the TIM II material was reapplied.

The first experiment was performed to determine the variability in Θ_{JC} measurements attributed to the test engineer. The initial Θ_{JC} testing procedure was simplified by preparing a testing kit and supplying it to each test engineer. The same heat sink, data acquisition system, instrumentation and calibration constants were shared among three different test engineers. Measurements for all devices under test (DUTs) were performed by three different test engineers. Measurements made by test engineer one and two were made in lab A and measurements made by a third engineer were made in lab B. Rather than reinstrument and recalibrate all packages, instrumentation and die calibrations developed by the first engineer were used by the second and third engineer. Also, the same test hardware and data acquisition system were utilized to make measurement by all other test engineers. CABGA Θ_{JC} data measured by the three different engineers are shown in Figure 4. The standard deviation in data measured for each package (3 samples corresponding to three test engineers) ranged between 1 to 7% of the average Θ_{JC} values. Measurements made for the TEPBGA2 are reported in Figure 5. High and low conductivity EMC were used in the assembly of TEPBGA2 packages. The embedded case thermocouples were used to make measurements for high conductivity EMC for TEPBGA2 packages 1, 2 and 6 while the heat-sink thermocouple method was used to measure Θ_{JC} for the low conductivity TEPBGA2 packages 3, 4, 5. The variation in data for the TEPBGA2 was lower than the CABGA package. The standard deviation was between 0.1 and 0.5% of the average Θ_{JC} values.

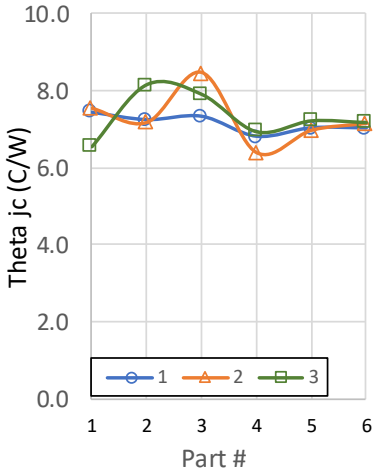

Figure 4. CABGA data comparison.

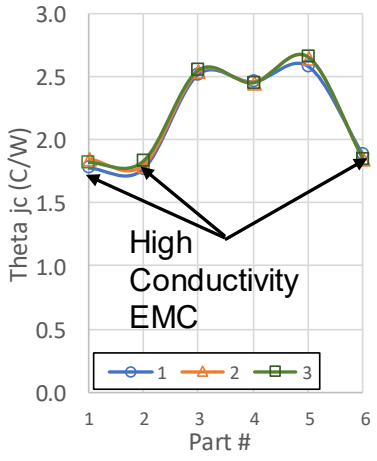

Figure 5. TEPBGA2 data comparison.

The last package tested was the FCBGA. Embedded thermocouples were used to sense the case temperature for all FCBGA packages tested. The standard deviation was approximately 1% for packages 1 – 5 whereas package 6 had a higher standard deviation, 8%, based on higher measurements made by engineer 3. In general, the agreement between data measured by three different engineers was acceptable using the same instrumentation, calibration and test setup.

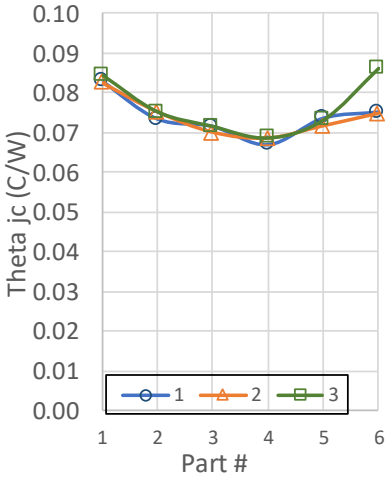

Figure 6. FCBGA data comparison.

The next step in determining the repeatability in measurement capability was to add the requirement that each engineer generate their own temperature sensor calibration and use a different data acquisition system. Two engineers in lab A and lab B gathered data using the same TTV for the each package, A5, B4 and C2 for CABGA, TEPBGA2 and FCBGA packages, respectively. These three TTVs were measured five times, each time removing it from the CPU cooler and reapplying the TIM II material. The data comparison is shown in Figure 7. The difference in data measured by engineer 1 and engineer 3 is less than 8%. It is believed that a lower difference in Θ_{JC} is possible if all data acquisition systems are calibrated using a common standard before measurements are made.

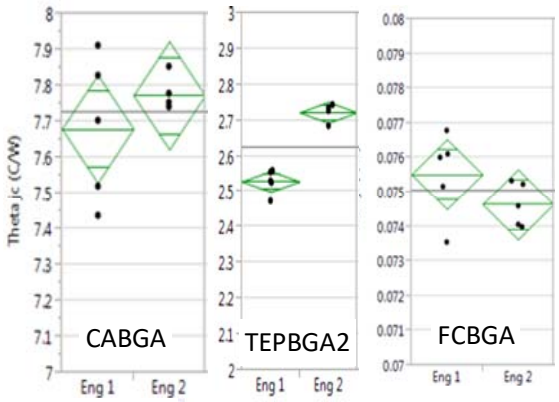

Figure 7. Repeatability study.

The next condition investigated was the effect of the heat-sink design and material on Θ_{JC} measurements. Six different heat-sink designs were tested; the standard CPU cooler used in previous tests, a water cooled cold plate, four different material plates mounted to a Θ_{JC} ring cold plate as shown in Figure 8. The plates were tested in order of decreasing thermal conductivity ranging from copper (k~390W/m/K), aluminum (k~180W/m/K), brass (k~110w/m/K) and steel (k~15W/m/K).

For these sets of experiments, engineer 1 performed all the testing using TTVs A5, B4 and C2 while switching out the interchangeable plate between tests. Test data were normalized by dividing the Θ_{JC} data for each TTV type by the CPU heat-sink Θ_{JC} data. Data from the heat-sink tests are shown in Figure 9. For the CABGA and TEPBGA2 TTVs, the impact of the CPU heat-sink was minimal. Lower power is required to keep the target ($T_j - T_c$) ~ 30°C as the thermal conductivity of the attached plate decreases from copper, to aluminum, to brass and lastly steel. It is possible to record a lower Θ_{JC} using a cold plate made from steel due to its higher spreading resistance. It is advisable to use high conductivity heat-sink materials to promote greater power dissipation thereby helping to reduce uncertainty in ΘJC measurements, see [6].

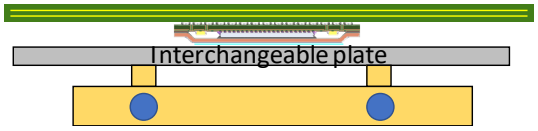

Figure 8. Heat sink variability fixture.

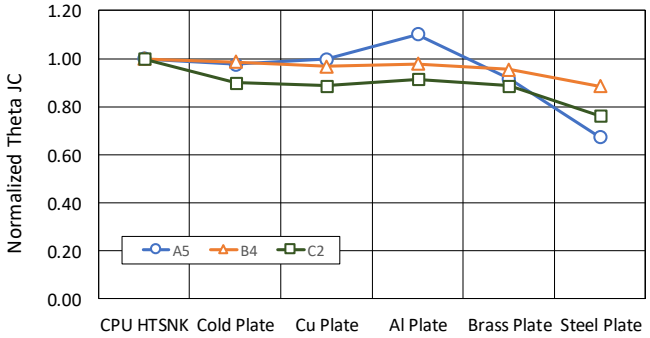

Figure 9. Effect of heat-sink design.

The last condition tested in this study was the Θ_{JC} variation caused by remounting the case thermocouple. TTV C6 was tested repeatedly. Between each test, the case thermocouple was removed and replaced with a new one and then calibrated. The variability in Θ_{JC} is shown in Figure 10 where the dashed lines representing ± 2 standard deviation about the mean.

For low Θ_{JC} measurements, improved methods are needed to attach thermocouples to reduce testing variation attributed to the mounting process.

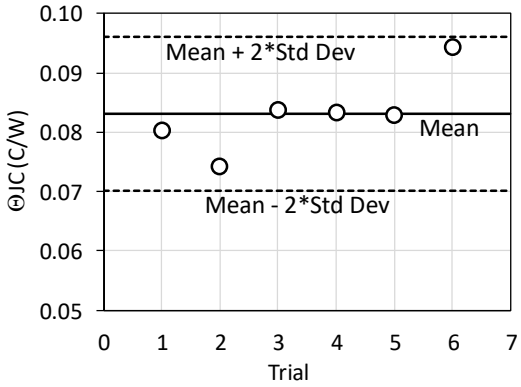

Figure 10. Θ_{JC} repeatability as a function of thermocouple attach trial.

3. Accurate Case Temperature Method

Simulations were used to specify the appropriate method for sensing case temperature. When possible, it is advisable to use the embedded thermocouple in the heat-sink to measure case temperature due to the consistency in making measurements with the same case temperature sensor and ease of use compared to embedding a thermocouple into the case for each individual package tested. For low Θ_{JC} applications, there is no choice. The resistance of the TIM II layer will be comparable to the Θ_{JC} of the package itself leading to large errors if the case temperature is measured with a thermocouple embedded into the heat-sink. A case temperature measurement guideline is needed to select the correct method for running Θ_{JC} tests.

If an uncertainty of 5% is acceptable in making Θ_{JC} measurements using the heat-sink mounted thermocouple, then the resistance contribution from the TIM II must be less than 5% of the value of Θ_{JC}.

$$\Theta TIM\ II \leq 0.05 * \Theta JC \qquad (2)$$

A limit can be written for the minimum Θ_{JC} heat-sink thermocouple configuration assuming the one-dimensional conduction relationship applies for predicting the resistance in the TIM II layer (ΘTIM II = $L/K_{TIMII}/A_{SPRD}$), where A_{SPRD} is the area in the TIM II layer experiencing heat flow. Note that A_{SPRD} will be larger than the die area.

$$\Theta JC * A_{SPRD} \geq 20 \frac{L}{K_{TIMII}} \qquad (3)$$

The definition for A_{SPRD} should be based on a physical model. The authors selected a simplified model based on the 45° spreading angle concept knowing full well that it is an approximation, see [7]. The spreading area available for heat transfer through the TIM II layer is calculated using equation (4), where S is the gap between the active surface of the die and the case.

$$A_{SPRD} = (L_{DIE} + 2S) * (W_{DIE} + 2S) \qquad (4)$$

It is possible to extend the range of applicability for smaller Θ_{JC} values using the embedded heat-sink thermocouple if the bond line (L) is reduced and/or the TIM II thermal conductivity (K_{TIMII}) is increased. Based on the thermal conductivity of the TIM II material used in this study, K_{TIMII}= 9W/m/K, and the assumed bond line thickness, 50μm, $\Theta_{JC} * A_{SPRD}$ must be larger than 110°C/Wmm^2.

The conduction path through the TIM II layer is not one-dimensional. It includes lateral spreading of heat from the die into adjacent materials and into materials above the die. There are many papers written on calculating the spreading resistance in electronics cooling applications, see for example [8]. The area available for spreading heat in the TIM II layer is larger than the area of the die. Three-dimensional affects must be analyzed using FEA simulations to predict the Θ_{JC} error associated with case temperatures made using an embedded thermocouple in the heat-sink.

Sample FEA simulations were run for the CABGA and FCBGA packages. For the CABGA package with a high Θ_{JC}, Θ_{JC} = 7.0°C/W, there is negligible temperature drop across the TIM II layer since the power level required to produce a junction temperature of approximately 55°C is small, see Figure 11. Hence resistance measured at the case, Θ_{JC}, or at the heat sink, Θ_{JS}, would give approximately the same value. Also note that the heat-flux ratio, defined as the heat-flux through the TIM II layer divided by the heat-flux at the active side of the die, is less than unity due to the spreading of heat laterally through the package. The heat-flux ratio is relatively flat over the die area and drops off outside of the die area.

When Θ_{JC} is low, the temperature drop across the TIM II layer is much larger. Consider the temperature across the TIM II layer for the FCBGA package when Θ_{JC} = 0.07°C/W, see Figure 12. The temperature drop across the TIM II layer is 5°C, approximately half the temperature drop predicted between the junction and case. Also note that the heat-flux ratio rises more sharply near the center of the package and falls of more quickly compared to the CABGA package.

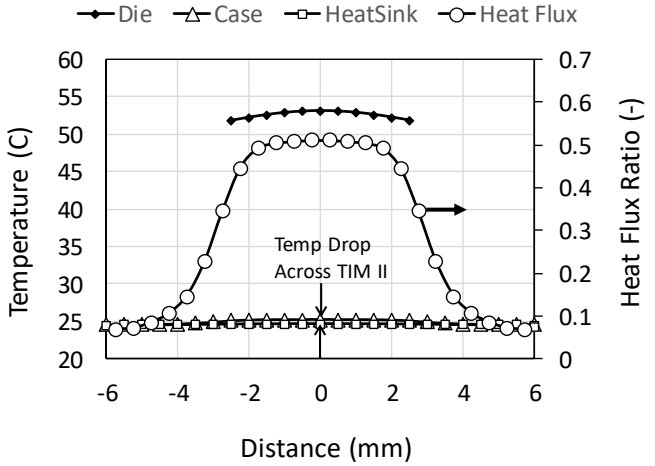

Figure 11. Heat spreading through TIM II layer for a 5mm die in a CAGA.

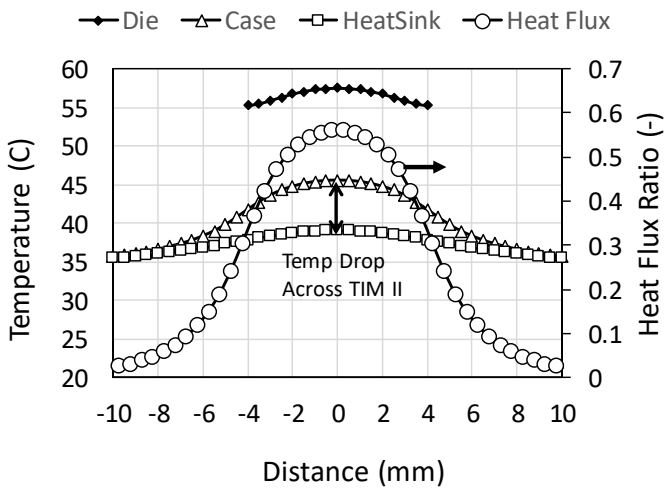

Figure 12. Heat spreading through TIM II layer for a 8mm die in a FCBGA.

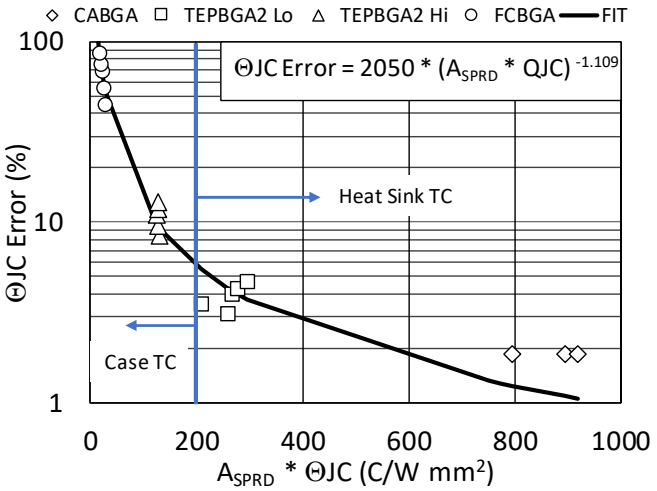

Figure 13. Predicted errors in ΘJC as a function of spreading area and ΘJC.

A more accurate method, than the one-dimensional analysis given in equation (3), is needed to decide what type of thermocouple should be used to measure the case temperature. The Θ_{JC} error, defined as $(\Theta_{JS} - \Theta_{JC})/ \Theta_{JC}$, was determined using FEA. When the error is larger than 5%, an embedded case thermocouple should be used.

Three different packages, shown in Table 1, were modeled to understand the dependency of the error in Θ_{JC} with A_{SPRD} for a range of die sizes, 3mm-9mm for CABGA, 4mm-14mm for TEPBGA2 and 6mm-20mm for FCBGA. The Θ_{JC} error was calculated based on the predicted junction and case temperatures at the center of the package, the heat flow through the TIM layer, Q, and the effective spreading area for the heat flow, A_{SPRD}, equation (4).

Results for CABGA, TEPBGA2 and FCBGA packages of varying die sizes are show in Figure 13. To achieve an error less than 5%, thermocouples should be embedded into the lid when $A_{SPRD}*\Theta_{JC}$ is less than 200C/Wmm^2. This critical value is greater than the value predicted by the one-dimensional flow case, equation (3). The FEA predictions reported in Figure 13 more accurately model the spreading resistance. An interesting result follows from these predictions. The TEPBGA2 with a higher thermal conductivity EMC requires an embedded thermocouple in its case whereas the lower thermal conductivity EMC version can be measured using a heat-sink mounted thermocouple.

4. Conclusions

Accurate Θ_{JC} measurements may be made by installing thermocouples into the heat-sink when $A_{SPRD}*\Theta_{JC}$ is greater than 200°C/Wmm^2. For $A_{SPRD}*\Theta_{JC}$ less than 200°C/Wmm^2, thermocouples must be installed into the case of the package. The repeatability in Θ_{JC} measurements was within 5% for most packages tested when the same data acquisition hardware was used. When measurements were repeated with data acquisition systems not traceable to the same standard, the difference increased to 8%.

References

1. JESD51-1, Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device), December 1995. https://www.jedec.org/standards-documents.
2. Galloway J. and Okpe T., "Challenges in Measuring Theta jc for High Thermal Performance Packages," Electronics Cooling Design, Number 2, Test & MeasurementTest & Measurement, Volume 20, May 29, 2014, https://www.electronics-cooling.com/2014/05/challenges-measuring-theta-jc-high-thermal-performance-packages/
3. Bernie Siegal, JEDEC meeting internal report presented at March 2007, JC15 Thermal Standards Meeting.
4. Lasance C. and Lacaze C, "A transient method for the accurate measurement of interface thermal resistances," Semiconductor Thermal Measurement and Management Symposium, 1996, SEMI-THERM XII Proceedings, pp. 43-50.
5. JESD51-14, "Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-To-Case of Semiconductor Devices with Heat Flow Through a Single Path," November 2010, https://www.jedec.org/standards-documents.
6. De Los Heros E., Galloway J., and Xu G., "Repeatable Surface Temperature Measurements Under High Heat Flux Conditions," Advanced Technology Workshop on Thermal Management, 2014, Los Gatos, CA.
7. Guenin Bruce, "The 45° Heat Spreading Angle – An Urban Legend?", November 1, 2003 Electronics Cooling, Standards, Test & Measurement, Volume 9, Number 4, https://www.electronics-cooling.com/2003/11/the-45-heat-spreading-angle-an-urban-legend
8. Schweitzer Dirk, "Effective heat spreading angle", September 15, 2015 Electronics Cooling, Semiconductor, Technical Brief, Volume 21 Number 3, https://www.electronics-cooling.com/2015/09/effective-heat-spreading-angle/#