

Heterogeneous Integration Using Organic Interposer Technology

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Abstract—As the costs of advanced node silicon have risen sharply with the 7 and 5-nanometer nodes, advanced packaging is coming to a crossroad where it is no longer fiscally prudent to pack all desired functionality into a single die. While single-die packages will still be around, the high-end market is shifting towards multiple-die packages to reduce overall costs and improve functionality. This shift is not just to add local memory, such as the addition of high-bandwidth memory (HBM) module(s) to an application-specific integrated circuit (ASIC) die, but also to separate what would have been a monolithic ASIC in prior generations to its constituent parts, such as the central processing unit (CPU) cores, serializer/deserializer (SerDes) and input/output (I/O) blocks. By splitting the monolithic die into smaller functional blocks, costs can be reduced through improved wafer yield on the smaller CPU cores and re-using older, vetted intellectual property (IP) from a prior silicon node for the I/O and SerDes that do not necessarily need the most advanced silicon node.

The traditional approach to fine-pitch multi-die packaging has been silicon interposers with Through Silicon Vias (TSVs). While the TSV approach has ushered in new performance levels never seen before, one of the major limitations is the inability to scale with higher and higher frequencies. The maximum frequency that a silicon interposer can handle between die-to-die interconnects is approximately 4 GHz due to the parasitics of the silicon. As die-to-die interconnects increase their bandwidth to higher and higher levels, the 4-6 GHz limitation can become a major bottleneck. Eliminating the silicon and silicon dioxide dielectrics and using polymers as the dielectric and the interposer itself can solve this problem.

This paper will discuss how to use High-Density Fan-Out (HDFO) technology to replace the TSV-bearing silicon interposer

with an organic interposer to enable higher bandwidth die-to-die interconnects for heterogeneous integration.

Keywords— *Heterogeneous integration, chip-last, RDL-first High-Density Fan-Out (HDFO), SWIFT®*

I. INTRODUCTION

The integrated circuit (IC) industry has moved boldly to 7 nm and 5-nm silicon technology nodes. However, wafer costs and design costs continue to increase exponentially, and power density is still increasing. Entire new product classes such as machine learning and deep neural networks are poised to dramatically alter technical innovation in every corner, from molecular modeling of new vaccines to new automated transportation paradigms for automobile travel and aircraft flight. This entire spectrum of new product innovations has one thing in common—an insatiable thirst for higher and higher compute performance, with nearly unimaginable data access and data throughput expectations. Indeed, it is an exciting and challenging time in the semiconductor industry.

To help with costs and ever shortening time to market (TTM) expectations, product designers are evaluating a broad portfolio of possible avenues to keep product performances increasing, rein in total product costs and reuse critical intellectual property (IP) blocks to shorten total development time. To that end, new silicon wafer nodes continue to produce performance increases, but in each, there are diminishing returns. Wafer costs are breathtaking, putting serious pressure towards minimizing the silicon area required for the latest and most expensive silicon node, ideally used only for those areas of a design where it is absolutely required to enable performance increases, such as

core computing, memory management and local memory caching. This means keeping die sizes in the latest node as small as possible. To enable this type of latest-generation silicon node economization, it must be technically and economically practical to build out the rest of the required functionality in previous-generation silicon nodes.

This trend towards heterogeneous integrations of different die originating from different silicon process nodes or even completely different substrate materials, e.g. silicon carbide or gallium arsenide, even functional sub-blocks of the system on chip (SoC) require new IC packaging approaches. In the 2011 and 2012 timeframes, the first 2.5D Through Silicon Via (TSV) products were introduced, principally to move dynamic random-access memory (DRAM) closer to the compute function [1], or to enable very-large die to be broken into sub-blocks for yield/cost/performance considerations [2]. The first discrete high-speed long reach serializer/deserializer (SerDes) input/output (I/O) chiplet devices became available 3 to 4 years ago. Now, product and IC architects have expanded to additional physical and electrical architectures with the chiplets and die-to-die interface requirements being quite varied, from short-reach serialized interfaces to wide, parallel interfaces.

Currently, there are two primary paths to achieve integration of heterogeneous die at the IC Package level, flip chip ball grid array (FCBGA) multichip modules (MCMs), where the diverse die are integrated directly at the package substrate level, or integrating the different die at a module level, and then attaching that module to the package substrate, using module technologies such as 2.5D TSV or High-Density Fan-Out (HDFO) integrations, see Fig. 1. The FCBGA MCM has been in production for decades and 2.5D TSV has been in production since 2012, while HDFO approaches have been available only recently.

Tradeoffs between these die-to-die interfaces is a current topic of design, development and standards bodies, with the goal of making these standard interfaces portable so that integrating IP blocks can use a standardized design flow. Standards bodies like the Open Domain Specific Architecture (ODSA) of the Open Compute Project (OCP) have been working to establish just such a common interface [3]. Physical routing densities and electrical performance both contribute to the selection of a suitable die-to-die interface.

This paper will explore the HDFO approach, known by the term Substrate SWIFT® (S-SWIFT) packaging in Amkor Technology, Inc.

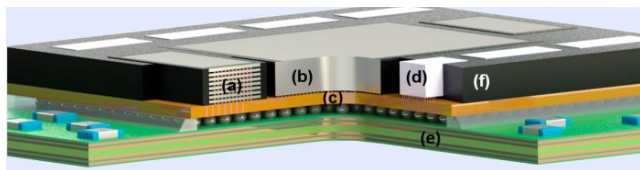


Fig. 1. (a) DRAM high-bandwidth memory (HBM), (b) application-specific integrated circuit (ASIC) or processor, (c) interposer (HDFO or 2.5D TSV), (d) discrete serializer/deserializer (SerDes) die, (e) laminate substrate, (f) epoxy mold compound (EMC).

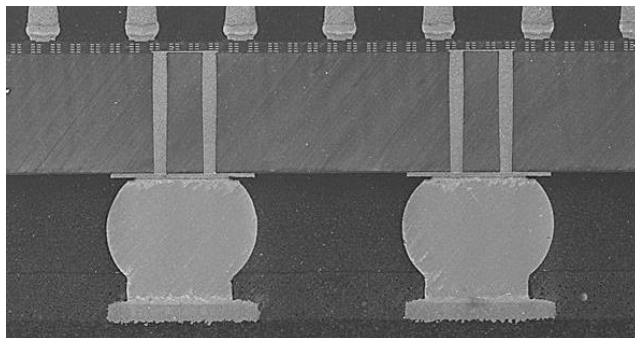


Fig. 2. 2.5D module with a TSV interposer cross section.

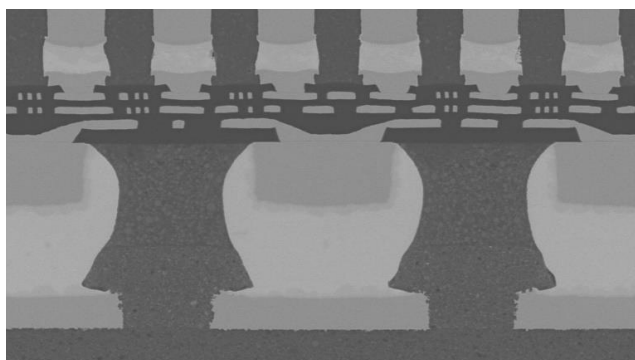


Fig. 3. Substrate SWIFT module SEM cross section.

II. CONSTRUCTION ANALYSIS

The standard TSV interposer is roughly 100- μm thick with typically 2-4 layers of copper (Cu) trace routing with silicon oxide as the dielectric on the front side with the fine-pitch interconnect and sometimes has a copper redistribution layer (RDL) on the back side with the coarser pitch interconnect, see Fig. 2. The SWIFT interposer has up to 4 layers of copper RDL with a polymer material as the dielectric. The thickness of the SWIFT interposer can range from 20 to 40 μm , see Fig. 3. The difference between the polymer and silicon oxide has significant impacts on the mechanical and electrical performance which will be detailed in Sections 4 and 5.

III. PROCESS FLOW

A. SWIFT Process Flow

The HDFO build-up process starts with a carrier. Several types of carriers, including glass, silicon and varying ceramics, have been tested and all have certain benefits and downsides. Glass carriers are readily available from multiple suppliers and come in several coefficients of thermal expansion (CTEs) ranging from 2 to 12 ppm/ $^{\circ}\text{C}$. Their modulus can also be adjusted to achieve different stiffnesses. Glass also has the benefit of being optically transparent, which allows laser debonding of the build-up structure. It also has the benefit of being able to be recycled. Silicon on the other hand does not share the modifiable CTE or modulus, nor is it optically transparent. The main benefits of silicon are that it is easy to source, matches the CTE of the die that is being attached and is cheaper than glass, although the cost benefit disappears if the glass can be reused. Ceramic carriers are more exotic but they

can offer similar benefits of glass. Although, in the ceramic carriers which were evaluated, there were no significant benefits to the glass carriers evaluated, therefore the cost was prohibitive.

The next process step depends on what type of carrier is chosen. If a glass carrier is used, the next process typically is the application of a separation layer to enable the release of the interposer workpiece (wafer or panel) at the end of the process. There are several different types of separation layers depending on how the release process is performed. There are several thermal and mechanical methods to perform carrier release but most recently laser release has become more of an industry standard. This has been due to the greater adoption of HBM modules which, until now, require the use of TSV interposers. The HBM's 55- μm bump pitch and signal requirements drive a 55- μm bump pad pitch and the use of 2- μm traces, which, until the adoption of HDFO processes, was not something the laminate substrate industry could support.

After the separation layer is applied, the build-up process truly begins. The first of several layers of polymer are applied, and typically when using round carriers, is spun-on. If a rectangular panel is used, it may be more economical that the polymer be applied via vacuum lamination, slit coating or sprayed-on. If the polymer has a photoinitiator, an ingredient that changes its properties when exposed to light, the next step is to image the desired pattern into the polymer. If there is no photoinitiator, then a photoresist sometimes needs to be applied prior to imaging. After imaging, if the photoinitiator is present, the next step is developing the material to remove the unwanted polymer. If no photoinitiator is used, an etch process must be used to remove the unwanted polymer. The etch process can be done using several methods, although the most popular are ultraviolet (UV) laser, excimer laser and reactive ion etch [4]. After etch, the photoresist is removed.

Once the desired portion of the polymer is removed, the first of several RDLs is deposited. The first step in this process is to apply a seed barrier layer using physical vapor deposition (PVD). The seed barrier layer has two major functions: to provide a conductive surface for plated copper and to roughen the surface to improve adhesion of the soon-to-be plated copper. The seed barrier layer could also be applied using an electroless plating process typical in laminate substrate manufacturing. After seed deposition, another photoresist is applied. As before, the photoresist is imaged and developed. Next, the copper is plated in the openings left in the photoresist. After plating, the photoresist is stripped from the surface. The now exposed seed layer where copper was not plated is removed. This is typically done with a wet chemical etch but recently a new method of removing the seed barrier layer with an excimer laser have been proved [5].

With the seed barrier layer removed, another layer of polymer is applied and the build-up process is repeated. This continues using the same process as detailed above until the last desired wiring layer is completed. Then, another layer of polymer is applied on top to seal it and vias are created on the top layer RDL via pads. Another seed barrier layer is deposited but instead of just plating copper, an under-bump metallurgy (UBM) is plated. This UBM is a stack of metals intended to protect the HDFO buildup from contamination by the tin in the

leadfree solder as well as to keep the surface solderable while in storage. Much of the HDFO process is now complete. What remains is Chip on Wafer (CoW) assembly similar to the CoW process used for TSV interposers.

B. CoW and FCBGA Assembly

The first step in the CoW process is flip chip attach and mass reflow. When using a glass carrier, the CTE mismatch between the glass and the silicon die can cause issues with warpage and misalignment of the bumps to pads. Depending on whether the CTE of the glass carrier is higher or lower than silicon, the design would need to apply either a shrink or growth factor. After reflowing, any flux residue is removed and then capillary underfill is dispensed and cured. The next step is overmolding the workpiece. Compression mold with liquid or granule epoxy mold compounds (EMC) is the most popular mold process used for wafer or panel sized carriers [3]. After the EMC has cured, the mold goes through a grinding process to expose the backside of the ASIC and HBM(s) for improved thermal performance. Next the first carrier is removed.

Carrier removal is highly dependent on the type of carrier used. Using a non-transparent carrier with a separation layer, mechanical or thermal debond are possible. If a non-transparent carrier is used without such a separation layer, the carrier must be removed by other means such as grinding, dry etch, wet etch or a combination of them. Transparent glass carriers make the carrier removal process much easier as a laser can shine through the carrier and affect the separation layer to be able to separate the carrier from the workpiece. Depending on the warpage of the workpiece without a carrier, it may be necessary to apply a second carrier to the exposed silicon and mold prior to the removal of the first carrier.

The workpiece then needs to be bumped with leadfree bumps or copper pillars. If a second carrier was added prior to the first carrier removal, it would be removed here and the workpiece transferred to dicing tape. Then the workpiece goes through a standard wafer or panel saw singulation process leaving individual modules. The individual modules are then transferred to a flipchip assembly line where the SWIFT modules can be handled like a silicon die or TSV CoW module and attached to a laminate substrate.

IV. MECHANICAL SIMULATION

Mechanical simulation can be used effectively as a tool to rapidly compare various geometries, components and materials without the cost of purchasing and building physical parts. Amkor Technology has used simulations for several years to specifically test and evaluate S-SWIFT HDFO structures and materials and compare S-SWIFT packaging with other technologies that serve the high-end advanced packaging market. See Fig. 4 for an example simulation comparison.

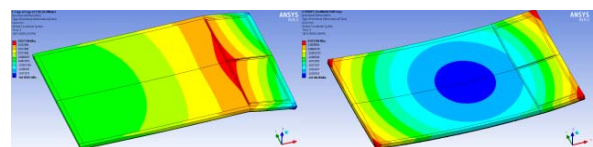


Fig. 4. Simulation of a live-bug view of warpage at reflow temperatures for 2.5D (left) vs. equivalent S-SWIFT (right) modules with 2 HBM devices. Note: sharp hinge and frowning-type warpage of 2.5D module.

A. Simulation Objective

A mechanical model was created to study the differences in warpage and stress between an Amkor S-SWIFT package with an ASIC and several HBMs, and an equivalent version of the same package with a 2.5D TSV interposer. The objective of the simulation effort presented in this paper was to compare mechanical shape change and mechanical stress due only to the material difference and thickness difference of the interposer itself. All other differences such as manufacturing process history were assumed to be less significant and were ignored.

The package that was studied in simulation was considered a virtual test-vehicle; no real-world counterpart was created (though similar packages may exist). The package has the following characteristics:

- Overall Package Dimensions: 68 mm x 68 mm x 3.1 mm.
- 1.7-mm thick 5-2-5 substrate, 120- μ m thick core, with typical FCBGA copper trace distribution through the trace layers.
- 25 mm x 35 mm ASIC and six HBM devices on a single module.
- 2.5D version: 100- μ m thick, with some RDL on top side and bump pads represented on bottom side.
- S-SWIFT version: 31- μ m thick, with 4 RDL layers with typical copper trace distribution.
- A relatively thin lid was used in the model.
- A typical FCBGA and S-SWIFT material set was used for this model with all materials except interposer material

These package choices will generally not affect comparative results when only one variable of interest is changed between Design of Experiment (DOE) legs.

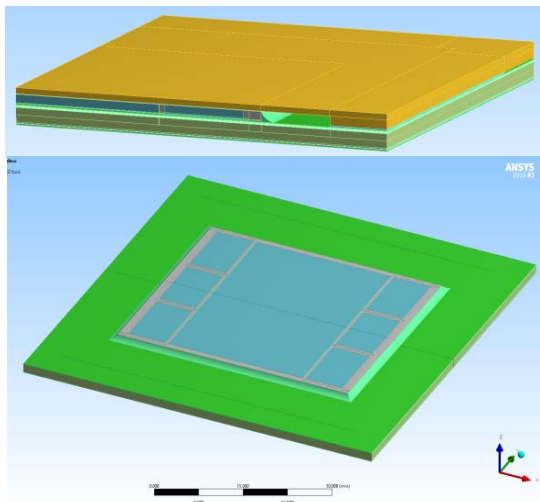


Fig. 5. Top – 3D view of quarter-symmetry model. Bottom – Expanded view of model, with lid hidden to view the module with ASIC and 6 HBM devices.

B. Model & Methodology

The model geometry was built in SolidWorks and translated into ANSYS Workbench Mechanical 2019 R3 using DesignModeler to refine and organize various model features. Several different parts were created and united with bonded contact elements in low-stress gradient areas to reduce the overall mesh count and increase model efficiency. Quarter-symmetry models between approximately 950 thousand and 1.5 million elements were used for these simulations (see Fig. 5 and Fig. 6).

Linear-elastic and temperature dependent material properties from supplier datasheets were used for the mechanical model. Object mass and weight were ignored, since the forces due to gravity at the package level (and below) are much smaller than the stiffness of the package. Perfect adhesion between materials was assumed and these simulations did not consider material degradation over time and over cyclic processes (such as thermal cycling). Copper trace material was randomly distributed across the appropriate model layers within the substrate and the interposer. Most bumps were ignored, since prior experience has shown that the underfill material itself provides enough structure to these mechanical models for reasonably accurate results for warpage. Several rows of simplified bumps were modeled near detailed bumps for stress modeling.

The models used a stress-free starting temperature of 150°C, with stress results measured at 20°C. Warpage was measured at room temperature and peak reflow temperature. The only items that were changed between 2.5D and S-SWIFT models were the thickness and material of the interposer itself.

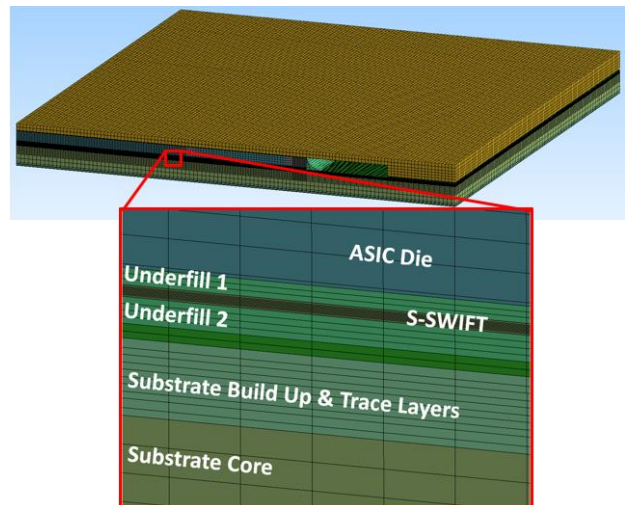


Fig. 6. Top – 3D view of quarter-symmetry model showing global model mesh. Bottom – detailed view of substrate, die and interposer layers for S-SWIFT version of the model.

C. Warpage

Module warpage is a critical factor in the package assembly process, since small solder bumps and copper pillars between the module and the substrate are very sensitive to the distance between their respective surfaces. Warpage magnitude at room-temperature for 2.5D modules is typically very low

(approximately 20 μm in this case) but the more critical reflow-temperature warpage magnitude can be much greater (about 70 μm in this simulation). The S-SWIFT module has greater room temperature warpage (about 60 μm), but less severe and more evenly distributed reflow-temperature warpage (about 40 μm). Module warpage from this simulation is presented below in Fig. 7.

Simulation was done to evaluate warpage of the package prior to lid attach (immediately after module attach and underfilling); results are reported in Fig. 8. Warpage in this case can be a good indicator of how much relative interaction there is between a die or module and substrate; for a given material set for a lidless package, increased warpage implies increased internal forces and more stress between a die and a substrate. Substrate SWIFT shows lower warpage prior to lid attach. In simulation this is due to more material compliance with the S-SWIFT layers versus the rigid layer of silicon in a 2.5D package.

Package warpage results are reported below in Fig. 9. Warpage magnitude and shape were similar between the 2.5D package and the S-SWIFT package. Overall warpage at both room- and reflow-temperature for this material set was approximately 20% higher for the S-SWIFT package but still within acceptable coplanarity ranges (< 200 μm for a 68-mm body size package). Note that the material set for this package had been optimized for 2.5D technology and was not changed for the S-SWIFT version in comparison. S-SWIFT designs typically have flatter module-area warpage and do not require exceptionally low CTE substrate materials to control package warpage. A significant driver of warpage for this specific simulation was the CTE mismatch between the copper lid and the chosen low-CTE substrate core material. Note that most warpage in the S-SWIFT device occurs outside the module area near the corner of this package.

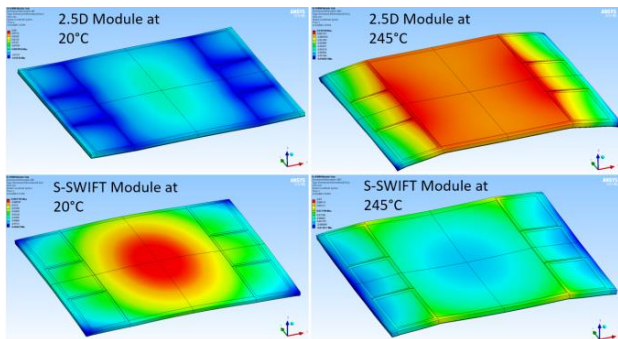


Fig. 7. Module warpage results from simulation (live-bug view). Color scale magnitudes are matched between top and bottom images. Note that warpage trends are opposite between 2.5D and S-SWIFT modules and the 2.5D module has much greater warpage magnitude and greater gradient (at HBM corners) than the equivalent S-SWIFT module.

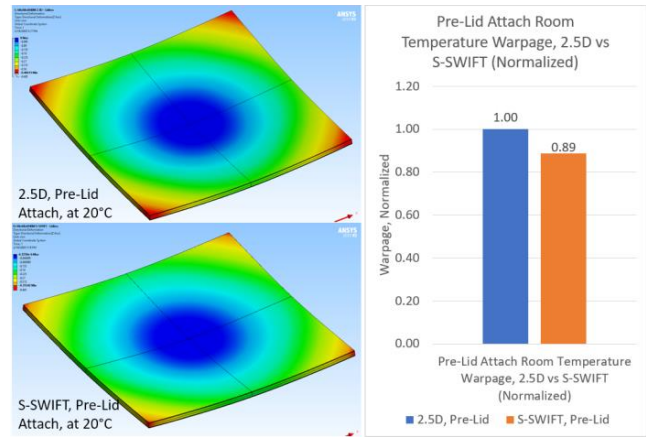


Fig. 8. Package warpage prior to lid-attach results from simulation (dead-bug view). Color scale magnitudes are matched.

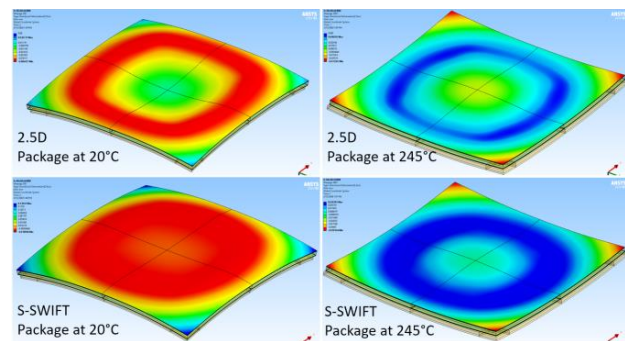


Fig. 9. Package warpage results from simulation after lid attach (dead-bug view). Color scale magnitudes are matched between top and bottom images.

D. Bump Stress & ASIC Stress

Once the package has been assembled, the stress within solder joints (an example of solder joint simulation in a S-SWIFT package is presented in Fig. 10) and at the active surface of the die become critical factors that determine longer term reliability and durability of the package. Generally, a lower-stressed joint will have a longer life and be less susceptible to fatigue and failure. It is also useful to compare stress within a known-good product technology such as 2.5D with a new technology such as S-SWIFT packages. If components in an S-SWIFT package are less stressed, it can be reasonable to expect similar or better life and reliability as the established 2.5D interposer technology.

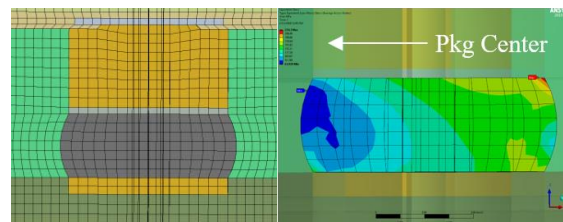


Fig. 10. Bump model mesh example and von Mises stress result for the ASIC corner bump in the S-SWIFT package.

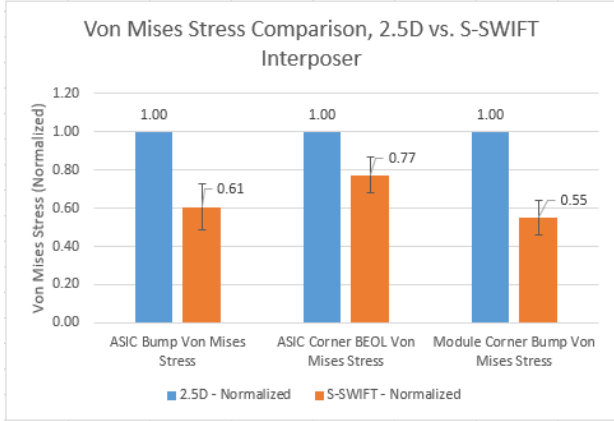


Fig. 11. Normalized result from stress modeling of critical bumps at the corner of the ASIC die and the corner of the module. Note significant reduction at all locations with S-SWIFT interposer. Error bars are from assumptions of high and low stiffness properties of S-SWIFT polymer.

Comparative results for stress at the corner ASIC joint (between die and interposer) and the corner module joint (between interposer and substrate) are reported in Fig. 11, along with a comparison of stress within the back end of line (BEOL) layers near the active surface of the ASIC. In all cases, the stress experienced by the joints and die is lower for the package with an S-SWIFT interposer. It was noted within the simulation environment that the S-SWIFT interposer is much more flexible and compliant than the equivalent 2.5D interposer, which may allow the S-SWIFT layers to better absorb and distribute stresses between the dies and the substrate.

E. Simulation Summary

Several key factors were studied in this simulation model. First, module warpage was observed in simulation to be much lower for an S-SWIFT module at reflow temperatures than an equivalent 2.5D module. The warpage gradient at the corners of the module was also much less severe than with a 2.5D module with HBM; this will reduce the risk of compressed bumps and bump shorting for solder joints near the corner of the module.

Second, package warpage magnitude and shape were similar between 2.5D and the equivalent S-SWIFT packages. Due to the difference between effective module CTE and stiffness, it may be prudent to choose slightly different lid or substrate core materials to optimize package shape and coplanarity; the same material set may not be appropriate for both 2.5D and S-SWIFT technologies.

Third, bump stress and die active-surface stress were significantly reduced with the S-SWIFT module in simulation.

V. ELECTRICAL SIMULATION

Selection of the proper die-to-die interface in heterogeneous package construction depends on two key factors: one, the number of physical wires per millimeter of die length between each pair of dies, and two, the electrical requirements of the die-to-die interface.

The number of physical wires is influenced heavily by the type of electrical interface selected, so these two factors are

strongly interrelated. Typical signal wire counts for FCBGA, the S-SWIFT package and 2.5D are found in Table 1

TABLE I. SIGNAL DENSITY IN DIFFERENT PACKAGE TYPES

Package Type	Signals per mm per layer	Trace/Space (μm)	Capture Pad (μm)
ABF Build-up	8-10	12/12	85
Substrate SWIFT	140-180	2/2	16
2.5D TSV	250-400	1/1	2

The wiring density is a function of both the signal width and space between traces (trace pitch) and the via sizes required to route from layer to layer. Silicon interposers using 65-nm Cu back-end of line (BEOL) technology are typically routed with signal pitches of 1 μm to 4 μm (0.5 μm line and space to 2 μm line and space). HDFO interposers are best suited to applications requiring 3 μm pitch to 10 μm pitch (1.5 μm line and space to 5 μm line and space).

The electrical performance of die-to-die interfaces depends on several key factors:

- Trace length
- Trace cross section
- Trace-to-trace spacing
- Ground reference scheme, e.g. strip-line, co-planar, combinations thereof, etc.
- Dielectric system
- Trace surface roughness when dealing with very high frequencies.

Electrical design starts by impedance matching to the I/O termination which can be achieved by proper geometric design, see Fig. 12. For example, the simple structures can be estimated with a simple equation, example shown below (1). Trace impedance is a function of the signal trace geometry, as well as the dielectric thickness and dielectric constant, ϵ_r .

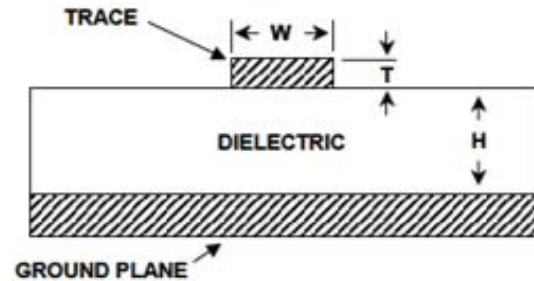


Fig. 12. Reference for Equation (1).

$$Z_0(\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \frac{5.98 \times H}{(0.8 \times W + T)} \quad (1)$$

For sophisticated high-speed designs, RF losses are the primary concern, since higher order harmonics become increasingly impactful at very high (gigabit/second) frequencies. In the frequency domain, the insertion loss accounts for both conductor and dielectric losses. An insertion loss comparison

between 2.5D and an S-SWIFT package is shown in Fig. 13. The polymer dielectric used in the S-SWIFT RDL has lower dielectric constant and, in particular, lower loss tangent (dissipation factor). In this analysis, 50-ohm structures were simulated in a strip line configuration over a waffle grid ground plane. As can be seen, the S-SWIFT package is quite linear and has significantly lower loss, especially at higher frequencies, relative to the 2.5D solution. This simulation used 4.5-mm trace lengths, typical in HBM or HBM2 routing. For other die-to-die interfaces, trace lengths will be shorter, even down to 0.8–1.0 mm in length.

In the time domain, Fig. 15 and Fig. 16 show eye-diagram comparisons. As expected, the eye height is significantly larger in the S-SWIFT case. For other die-to-die interfaces, signal wire length will be shorter than those for HBM memory data bus. This in turn, lowers the insertion loss accordingly. Fig. 14 shows this effect for several trace lengths, with 2 μm wide x 4 μm tall traces and 5 μm spacing, using microstrip construction. This low loss demonstrates the ability for S-SWIFT to address much higher communication speeds, especially when die to die spacing is small and signal lengths are shorter. It is not uncommon for the I/O driver sections of adjacent dies to be less than 500 or 600 microns long.

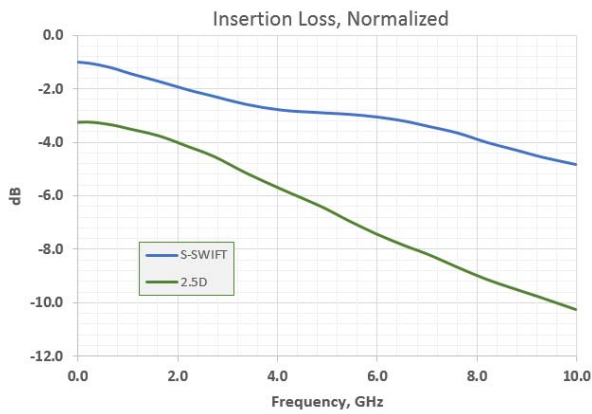


Fig. 13. Insertion loss comparison between 2.5D silicon Interposer and Substrate SWIFT RDL.

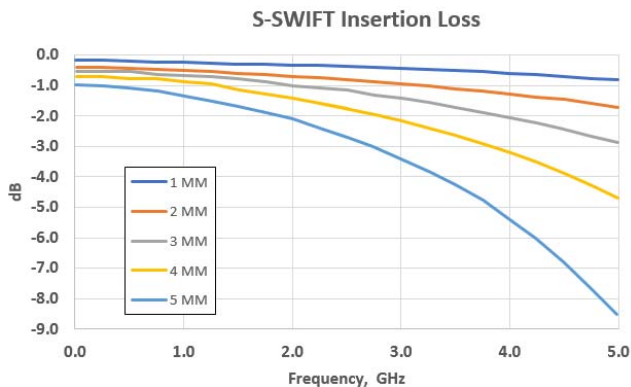


Fig. 14. S-SWIFT insertion loss vs. frequency for different trace lengths.

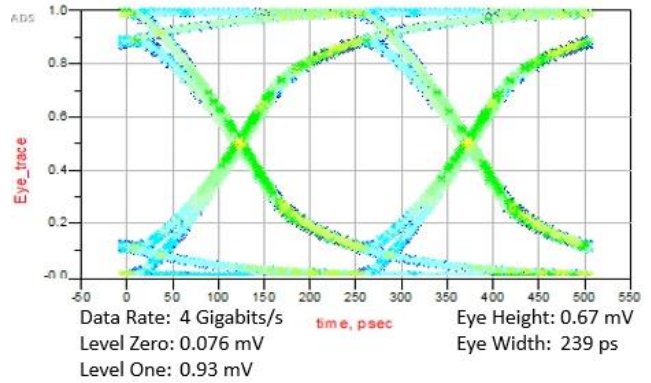


Fig. 15. Substrate SWIFT eye diagram.

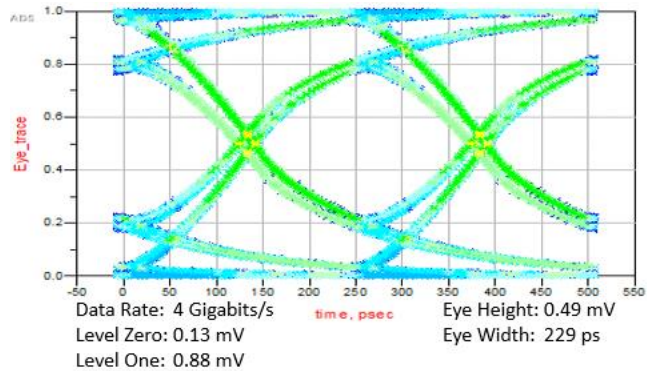


Fig. 16. 2.5D TSV silicon interposer eye diagram.

VI. RELIABILITY PERFORMANCE

To evaluate the reliability of S-SWIFT package, a test vehicle was designed and fabricated with 4 layers of RDL and a daisy chain in 67.5-mm x 67.5-mm package body size. The reliability tests were performed in accordance with the JEDEC standard including moisture soaking level 4 (MSL4) as precondition [7], temperature cycling test (TCT) with -40°C to 125°C / 1000 cycles (condition G) and unbiased high accelerated stress test (UHAST) with 110°C /264 hours. The high temperature storage test (HTS) with 150°C /1000 hours was also evaluated. Package integrity was monitored before and after reliability tests as well as daisy chain connectivity by checking the resistance. Daisy chain resistance increases by 20% are considered as an electrical test (ET) failure. Table 2 presents the results of package-level reliability test. All samples passed the reliability tests.

Fig. 17 presents cross-sectional images of microbump from end-of-line (EOL) and post reliability tests. The section position is 2- μm line/space RDL area. The bump diameter is 25 μm and bump pitch 45 μm . No solder joint failures were found and all reliability tests were passed.

TABLE II. RELIABILITY TEST RESULTS FROM PACKAGE LEVEL TESTING

Test Item	Conditions	Read Point	Sample Size	Result
MSL4	30°C / 60%RH 245°C x3	Precon	50	Pass
T/C G	-40°C to 125°C	1000 cycles	25	Pass
uHAST	110°C/85%RH	264 hours	25	Pass
HTS	150°C	1000 hours	25	Pass

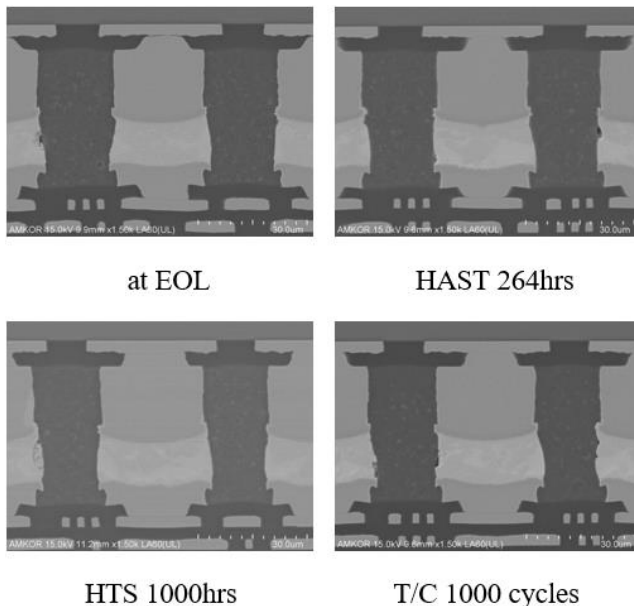


Fig. 17. Cross-section images of micro bump as EOL after reliability tests.

VII. CONCLUSIONS

Both in simulations and test vehicle results, Substrate SWIFT packaging has demonstrated excellent electrical performance and mechanical robustness. This robustness has also been demonstrated with large body test vehicles, as previously discussed, largely by the reduction in stress imparted on the die. The improved electrical performance will provide a reliable platform for die-to-die bus speeds well beyond that now required by HBM2 and HBM2e enabling Substrate SWIFT packaging to serve both the ASIC-HBM configuration as well as the many and varied chiplet-based constructions now in the marketplace and on the drawing board.

ACKNOWLEDGMENT

The authors would like to thank Alex Copia, Tyler Koenig, Moh Kolbehdari, and Ruben Fuentes from Amkor's Tempe, Arizona Design Center and TaeKi Kim and JiYeon Ryu, from Amkor's Incheon, Korea K5 facility for their design and simulation support. The authors would also like to thank MinJae Yi, SangHyouon Lee, and WonChul Do from Amkor's Incheon, Korea K5 facility for their assistance in processing and assembly support. Finally, the authors would like to thank Ron Huemoeller and JinYoung Khim, from Amkor's executive management team for their leadership and vision in pursuing Substrate SWIFT packaging technology.

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